ORCA® ORLI10G Field-Programmable System Chip 10 Gbits/s Transmit and Receive Line Interface

Introduction

Agere Systems Inc has developed a new *ORCA* Series 4 based FPSC, which combines a high-speed line interface with a flexible FPGA logic core. Built on the Series 4 reconfigurable embedded system-on-chips (SoC) architecture, the ORLI10G consists of an OIF standard (OIF 99.102.5) compliant XSBI 10 Gbits/s transmit and 10 Gbits/s receive line interface. Both transmit and receive interfaces consist of 16-bit LVDS data up to 667 Mbits/s, integrated transmit and receive programmable PLLs for data rate conversions between the line-side and system-side data rates, and a programmable logic interface at the system end for use with SONET/SDH, Ethernet, or OTN/digital wrapper with strong FEC system device data standards. In addition to the embedded functionality, the device will include up to 400k of usable FPGA gates. The line interface includes logic to divide the data rate down to 167 MHz or less (1/4 line rate) or 84 MHz or less (1/8 line rate) for transfer to the FPGA logic. The ORLI10G is designed to connect directly to Lucent's 10 Gbits/s TTRN0110G MUX and TRCV0110G deMUX on the line side as well as other industry-standard devices. The programmable logic interface on the system side allows for direct connection to a 10 Gbits/s Ethernet MAC, a 10 Gbits/s SONET/SDH framer/data engine, or a 10 Gbits/s digital wrapper/FEC framer/data engine.

For 10 Gbits/s Ethernet, the ORLI10G supports the physical coding sublayer (PCS), interfaces to the physical media attachment (PMA), and connects to the system interface (host or switch) for the proposed *IEEE** 802.3ae 10 Gbits/s serial LAN PHY.

The ORLI10G FPSC is a high-speed programmable device for 10 Gbits/s data solutions. It can be used as the interface between the line interface and the system interface in a variety of emerging networks, including 10 Gbits/s SONET/SDH (OC-192/STM-48), 10 Gbits/s optical transport networks (OTN) using digital wrapper and strong FEC, or 10 Gbits/s Ethernet. Other functions include use in Quad OC-48/STM-16 SONET/SDH systems, interfaces between Quad OC-48/STM-16 and OC-192/STM-64 components, and use as a generic data transfer mechanism between two devices at 10 Gbits/s rates. Data is received at the line interface and then sent to either a 4-bit or 8-bit serial-to-parallel converter. On the transmit interface, either a 4-bit or 8-bit parallel-to-serial converter is used. Thus, the data rate at the internal FPGA interface is either 1/4 or 1/8 the line rate.

The programmable PLLs on the ORLI10G provide for great flexibility in handling clock rate conversion due to differing amounts of overhead bits in various system data standards. For example, when used as a 10 Gbits/s Ethernet interface, the ORLI10G will automatically divide the line frequency of 645 MHz by 4 x 66/64 (receive side) to synchronize with the system frequency of 156 MHz. When the ORLI10G is used as an interface to a 10 Gbits/s digital wrapper/FEC framer/data engine, these same PLLs can divide the strong FEC standard line frequency of 667 MHz by 4 x 15/14 (receive side) to provide the 156 MHz system clock frequency. The ORLI10G can also divide down the STS-192/STM-64 SONET/SDH data line rate of 622 MHz by 4 to synchronize with a 155 MHz system clock. The ORLI10G can also be configured to provide a 78 MHz system data rate.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. *ORCA* ORLI10G—Available FPGA Logic

Device	PFU Rows	PFU Columns	Total PFUs	User I/Os	LUTs	EBR Blocks	EBR Bits (k)	Usable Gates (k)
ORLI10G	36	36	1296	432	10368	12	111	380—800

† The embedded core and interface are not included in the above gate counts. The usable gate counts range from a logic-only gate count to a gate count assuming 20% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit plus each block has an additional 25k gates. 7k gates are used for each PLL and 50k gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate count calculations.

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Embedded Function Features

- Provides a 10 Gbits/s line interface-to-interface with various system standards such as OC-192/STM-64 SONET/SDH, Quad OC-48/STM-16 10 Gbits/s Ethernet, and 10 Gbits/s OTN (digital wrapper/strong FEC).
- Embedded PLLs with programmable M/N multiplication/division values provide for flexible data rate conversion between line side and system side.
- Line side provides for 16-bit LVDS data with multiple line frequencies supported up to 667 MHz.
- Line-side interface, including timing and jitter specifications, compliant to OIF 99.102.5 standard.
- Receive-side interface can be split into four separate asynchronous 2.5 Gbits/s interfaces (4-bit LVDS data interface for each) with a separate clock for each for transfer to the FPGA logic.
- Data and clock rates divided by 4 or 8 for use in FPGA logic.
- Direct interface to Lucent's 10 Gbits/s MUX (TTRN0110G) and deMUX (TRCV0110G).
- LVDS I/Os compliant with *EIA**-644, support hot insertion. All embedded LVDS I/Os include both input and output on-board termination to allow high-speed operation.
- Low-power LVDS buffers.
- Built-in boundary scan (*IEEE* 1149.1 JTAG).

Intellectual Property Features

Programmable logic provides a variety of yet-to-be standardized interface functions, including the following IP core functions:

- 10 Gbits/s Ethernet as defined by *IEEE* 802.3ae:
  - — XGMII for interfacing to 10 Gbits/s Ethernet MACs. XGMII is a 156 MHz double data rate parallel short-reach (typically less than 2 inches) interconnect interface.
  - — Elastic store buffers for clock domain transfer to/from the XGMII interface.
  - — $X^{58} + X^{19} + X^{1}$ scrambler/descrambler for 10 Gbits/s Ethernet.
  - — 66-bit word aligner and 64b/66b receive path decoder, 64b/66b transmit path encoder, and 66b/64b transmit path conversion for Ethernet overhead bits.
  - — 10 Gbits/s media access controller (MAC) can be implemented in a separate FPGA, FPSC, or ASIC.
- POS-PHY4 interface for 10 Gbits/s SONET/SDH and OTN systems and some 10 Gbits/s Ethernet systems.
- Quad 2.5 Gbits/s SONET/SDH to 10 Gbits/s SONET/SDH MUX/deMUX functions.

Programmable Features

- High-performance programmable logic:
  - — 0.13 µm 7-level metal technology.
  - — Internal performance of >250 MHz.
  - — 400k usable system gates.
  - — Meets multiple I/O interface standards.
  - — 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - — LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - — Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - — Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - — Two slew rates supported (fast & slew-limited).
  - — Fast-capture input latch and input flip-flop (FF) latch for reduced input setup time and zero hold time.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
  - — Off-chip clock drive capability.
  - — Two input function generator in output path.
- New programmable high-speed I/O:
  - — Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I & II), HSTL (Class I, III, IV), ZBT, and DDR.
  - — Double-ended: LVDS, bused-LVDS, LVPECL.
  - — Customer defined: ability to substitute arbitrary standard-cell I/O to meet fast moving standards.
- New capability to (de)multiplex I/O signals:
  - — New DDR on both input and output at rates up to 311 MHz (622 MHz effective rate).
  - — New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).

* *EIA* is a registered trademark of Electronic Industries Association.

Programmable Features (continued)

- Enhanced twin-quad programmable function unit (PFU):
  - — Eight 16-bit look-up tables (LUTs) per PFU.
  - — Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - — New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - — New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - — 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - — Flexible fast access to PFU inputs from routing.
  - — Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also allows many I/O specifications to be met for setup/hold and clock-to-out times. It may also reduce ground bounce effects for output buses by allowing flexible delays in switching output buffers.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and *PAL**-like and-or-invert (AOI) in each programmable logic cell.
- New 200 MHz embedded quad-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:
  - — One—512 x 18 (quad-port, two read/two write) with optional built-in arbitration.
  - — One—256 x 36 (dual-port, one read/one write).
  - — One—1k x 9 (dual-port, one read/one write).
  - — Two—512 x 9 (dual-port, one read/one write for each).
  - — Two RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - — Supports joining of RAM blocks.
  - — Two 16 x 8-bit content addressable memory (CAM) support.
  - — FIFO 512 x 18, 256 x 36, 1k x 9, or dual 512 x 9.
  - — Constant multiply (8 x 16 or 16 x 8).
  - — Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard-cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - — Full boundary scan (*IEEE* 1149.1 and draft 1149.2 JTAG).
  - — Programming and readback through boundary-scan port compliant to *IEEE* Draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provides optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz.

* *PAL* is a trademark of Advanced Micro Devices, Inc.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC**860 and *PowerPC* II high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard-cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA*† specification 2.0 AHB system bus (*ARM* † processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard-cell blocks.
- New network PLLs meet ITU-T G.811 specifications and provide clock conditioning for DS-1/E-1 and STS-3/STM-1 applications.
- Flexible general-purpose PPLLs offer clock multiply (up to 8x), divide (down to 1/8x), phase shift, delay compensation, and duty-cycle adjustment combined.
- Variable-size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to seven high-speed clocks on each edge of the device for improved setup/hold times on input pins and clock-to-out times on output pins (and both improvements for bidirectional pins).
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced-speed internal logic.
- *ORCA* Foundry development system software. Supported by industry standard.
- CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets universal test and operations PHY interface for ATM (UTOPIA) Levels 1, 2, and 3 as well as POS-PHY3. Also meets proposed specifications for UTOPIA Level 4 and POS-PHY4 for 10 Gbits/s interfaces.
- Meets POS-PHY3 (2.5 Gbits/s) and POS-PHY4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.

* *PowerPC* is a registered trademark of International Business Machines, Inc.
† *AMBA* is a trademark and *ARM* is a registered trademark of Advanced RISC Machines Limited.

Description

FPSC Definition

FPSCs, or field-programmable system chips, are devices that combine field-programmable logic with ASIC or mask-programmed logic on a single device. FPSCs provide the time to market and the flexibility of FPGAs, the design effort savings of using soft intellectual property (IP) cores, and the speed, design density, and economy of ASICs.

FPSC Overview

Lucent's Series 4 FPSCs are created from Series 4 *ORCA* FPGAs. To create a Series 4 FPSC, several columns of programmable logic cells (see FPGA Logic Overview section for FPGA logic details) are added to an embedded logic core. Other than replacing some FPGA gates with ASIC gates, at greater than 10:1 efficiency, none of the FPGA functionality is changed—all of the Series 4 FPGA capability is retained: embedded block RAMs, MPI, PCMs, boundary scan, etc. The columns of programmable logic are replaced at the right of the device, allowing pins from the replaced columns to be used as I/O pins for the embedded core. The remainder of the device pins retain their FPGA functionality.

The embedded cores can take many forms and generally come from Lucent Technologies ASIC libraries. Other offerings allow customers to supply their own core functions for the creation of custom FPSCs.

FPSC Gate Counting

The total gate count for an FPSC is the sum of its embedded core (standard-cell/ASIC gates) and its FPGA gates. Because FPGA gates are generally expressed as a usable range with a nominal value, the total FPSC gate count is sometimes expressed in the same manner. Standard-cell ASIC gates are, however, 10 to 25 times more silicon-area efficient than FPGA gates. Therefore, an FPSC with an embedded function is gate equivalent to an FPGA with a much larger gate count.

FPGA/Embedded Core Interface

The interface between the FPGA logic and the embedded core has been enhanced to allow for a greater number of interface signals than on previous FPSC architectures. Compared to bringing embedded core signals off-chip, this on-chip interface is much faster and requires less power. All of the delays for the interface are precharacterized and accounted for in the *ORCA* Foundry Development System.

Series 4 based FPSCs expand this interface by providing a link between the embedded block and the multimaster 32-bit system bus in the FPGA logic. This system bus allows the core easy access to many of the FPGA logic functions including the embedded block RAMs and the microprocessor interface.

Clock spines also can pass across the FPGA/embedded core boundary. This allows for fast, low-skew clocking between the FPGA and the embedded core. Many of the special signals from the FPGA, such as DONE and global set/reset, are also available to the embedded core, making it possible to fully integrate the embedded core with the FPGA as a system.

For even greater system flexibility, FPGA configuration RAMs are available for use by the embedded core. This allows for user-programmable options in the embedded core, in turn allowing for greater flexibility. Multiple embedded core configurations may be designed into a single device with user-programmable control over which configurations are implemented, as well as the capability to change core functionality simply by reconfiguring the device.

ORCA Foundry Development System

The *ORCA* Foundry development system is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture and then place and route it using *ORCA* Foundry's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The *ORCA* Foundry development system interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow: design entry and the bitstream generation stage. Recent improvements in *ORCA* Foundry allow the user to provide timing requirement information through logical preferences only; thus, the designer is not required to have physical knowledge of the implementation.

Description (continued)

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. A floorplanner is available for layout feedback and control. A static timing analysis tool is provided to determine design speed, and a back-annotated netlist can be created to allow simulation and timing.

Timing and simulation output files from *ORCA* Foundry are also compatible with many third-party analysis tools. A bit stream generator is then used to generate the configuration data which is loaded into the FPGAs internal configuration RAM, embedded block RAM, and/or FPSC memory.

When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, *ORCA* Foundry produces configuration data that implements the various logic and routing options discussed in this data sheet.

FPSC Design Kit

Development is facilitated by an FPSC design kit which, together with *ORCA* Foundry and third-party synthesis and simulation engines, provides all software and documentation required to design and verify an FPSC implementation. Included in the kit are the FPSC configuration manager, *Synopsys Smart Model**, and complete online documentation. The kit's software couples with *ORCA* Foundry, providing a seamless FPSC design environment. More information can be obtained by visiting the *ORCA* website or contacting a local sales office, both listed on the last page of this document.

FPGA Logic Overview

The *ORCA* Series 4 architecture is a new generation of SRAM-based programmable devices from Lucent Technologies Microelectronics Group. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable system-on-chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: programmable logic cells (PLCs), programmable I/O cells (PIOs), embedded block RAMs (EBRs), and system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs are surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core. Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals. Large blocks of 512 x 18 quad-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MPI, PLLs, and the embedded system bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/FFs, and one additional flip-flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion; two sets of four LUTs and FFs that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

* *Synopsys Smart Model* is a registered trademark of Synopsys, Inc.

Description (continued)

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous *ORCA* devices, with the additional new features which allow the user the flexibility to select new I/O types that support high-speed interfaces.

Each PIO contains four programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local set/reset, and global set/reset. On the input side, each PIO contains a programmable latch/flip-flop which enables very fast latching of data from any pad. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU.

On the output side of each PIO, an output from the PLC array can be routed to each output flip-flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The output buffer signal can be inverted, and the 3-state control can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered.

The Series 4 I/O logic has been enhanced to include modes for speed uplink and downlink capabilities. These modes are supported through shift register logic, which divides down incoming data rates or multiplies up outgoing data rates. This new logic block also supports high-speed DDR mode requirements where data is clocked into and out of the I/O buffers on both edges of the clock.

The new programmable I/O cell allows designers to select I/Os which meet many new communication standards permitting the device to hook up directly without any external interface translation. They support traditional FPGA standards as well as high-speed, single-ended, and differential-pair signaling (as shown in Table 1). Based on a programmable, bank-oriented I/O ring architecture, designs can be implemented using 3.3 V, 2.5 V, 1.8 V, and 1.5 V referenced output levels.

Routing

The abundant routing resources of the Series 4 architecture are organized to route signals individually or as buses with related control signals. Both local and global signals utilize high-speed buffered and nonbuffered routes. One PLC segmented (x1), six PLC segmented (x6), and bused half chip (xHL) routes are patterned together to provide high connectivity with fast software routing times and high-speed system performance.

Eight fully distributed primary clocks are routed on a low-skew, high-speed distribution network and may be sourced from dedicated I/O pads, PLLs, or the PLC logic. Secondary and edge-clock routing is available for fast regional clock or control signal routing for both internal regions and on device edges. Secondary clock routing can be sourced from any I/O pin, PLLs, or the PLC logic.

The improved routing resources offer great flexibility in moving signals to and from the logic core. This flexibility translates into an improved capability to route designs at the required speeds when the I/O signals have been locked to specific pins.

System-Level Features

The Series 4 also provides system-level functionality by means of its microprocessor interface, embedded system bus, quad-port embedded block RAMs, universal programmable phase-locked loops, and the addition of highly tuned networking specific phase-locked loops. These functional blocks allow for easy glueless system interfacing and the capability to adjust to varying conditions in today's high-speed networking systems.

Microprocessor Interface

The MPI provides a glueless interface between the FPGA and *PowerPC* microprocessors. Programmable in 8-, 16-, and 32-bit interfaces with optional parity to the *Motorola* PowerPC* 860 bus, it can be used for configuration and readback, as well as for FPGA control and monitoring of FPGA status. All MPI transactions utilize the Series 4 embedded system bus at 66 MHz performance.

A system-level microprocessor interface to the FPGA user-defined logic following configuration, through the system bus, including access to the embedded block RAM and general user-logic, is provided by the MPI. The MPI supports burst data read and write transfers, allowing short, uneven transmission of data through the interface by including data FIFOs. Transfer accesses can be single beat (1 x 4 bytes or less), 4-beat (4 x 4 bytes), 8-beat (8 x 2 bytes), or 16-beat (16 x 1 bytes).

System Bus

An on-chip, multimaster, 8-bit system bus with 1-bit parity facilitates communication among the MPI, configuration logic, FPGA control, and status registers, embedded block RAMs, as well as user logic. Utilizing the *AMBA* specification Rev 2.0 AHB protocol, the embedded system bus offers arbiter, decoder, master, and slave elements.

The system bus control registers can provide control to the FPGA such as signaling for reprogramming, reset functions, and PLL programming. Status registers monitor INIT, DONE, and system bus errors. An interrupt controller is integrated to provide up to eight possible interrupt resources. Bus clock generation can be sourced from the microprocessor interface clock, configuration clock (for slave configuration modes), internal oscillator, user clock from routing, or from the port clock (for JTAG configuration modes).

* *Motorola* is a registered trademark of Motorola, Inc.

Phase-Locked Loops

Up to eight PLLs are provided on each Series 4 device, with four PLLs generally provided for FPSCs. Programmable PLLs can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Each PPLL is capable of manipulating and conditioning clocks from 20 MHz to 420 MHz. Frequencies can be adjusted from 1/8x to 8x, the input clock frequency. Each programmable PLL provides two outputs that have different multiplication factors but can have the same phase relationships. Duty cycles and phase delays can be adjusted in 12.5% of the clock period increments. An automatic input buffer delay compensation mode is available for phase delay. Each PPLL provides two outputs that can have programmable (12.5% steps) phase differences.

Additional highly tuned and characterized, dedicated phase-locked loops (DPLLs) are included to ease system designs. These DPLLs meet ITU-T G.811 primary-clocking specifications and enable system designers to very tightly target specified clock conditioning not traditionally available in the universal PPLLs. Initial DPLLs are targeted to low-speed networking DS1 and E1, and also high-speed SONET/SDH networking STS-3 and STM-1 systems.

Embedded Block RAM

New 512 x 18 quad-port RAM blocks are embedded in the FPGA core to significantly increase the amount of memory and complement the distributed PFU memories. The EBRs include two write ports, two read ports, and two byte lane enables which provide four-port operation. Optional arbitration between the two write ports is available, as well as direct connection to the high-speed system bus.

Additional logic has been incorporated to allow significant flexibility for FIFO, constant multiply, and two-variable multiply functions. The user can configure FIFO blocks with flexible depths of 512k, 256k, and 1k including asynchronous and synchronous modes and programmable status and error flags. Multiplier capabilities allow a multiple of an 8-bit number with a 16-bit fixed coefficient or vice versa (24-bit output), or a multiply of two 8-bit numbers (16-bit output). On-the-fly coefficient modifications are available through the second read/write port. Two 16 x 8-bit CAMs per embedded block can be implemented in single match, multiple match, and clear modes. The EBRs can also be preloaded at device configuration time.

System-Level Features (continued)

Configuration

The FPGAs functionality is determined by internal configuration RAM. The FPGAs internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The configuration data can reside externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin-count method for configuring FPGAs.

The RAM is loaded by using one of several configuration modes. Supporting the traditional master/slave serial, master/slave parallel, and asynchronous peripheral modes, the Series 4 also utilizes its microprocessor interface and embedded system bus to perform both programming and readback. Daisy chaining of multiple devices and partial reconfiguration are also permitted.

Other configuration options include the initialization of the embedded-block RAM memories and FPSC memory as well as system bus options and bit stream error checking. Programming and readback through the JTAG *(IEEE* 1149.2*)* port is also available meeting in-system programming (ISP) standards (*IEEE* 1532 Draft).

Additional Information

Contact your local Lucent Technologies representative for additional information regarding the *ORCA* Series 4 FPGA devices, or visit our website at:
http://www.lucent.com/micro/netcom/orca

ORLI10G Overview

Device Layout

The ORLI10G FPSC provides a high-speed transmit and receive line interface combined with FPGA logic. The device is based on the 1.5 V OR4E4 FPGA. The ORLI10G consists of an embedded backplane transceiver core and a full OR4E4 36x36 FPGA array.

The ORLI10G is a line interface device that contains an FPGA base array, a 10 Gbits/s Line Interface block and programmable PLLs to do the overhead clock rate conversions on a single monolithic chip. The embedded portion includes:

Line Interface: This consists of a 16-bit LVDS receive data bus and a 16-bit LVDS transmit bus operating up to 667 Mbits/s per input/output pair. Each 4-bit LVDS I/O has a high-speed LVDS clock (operating up to 667 MHz) associated with it.

MUX/deMUX: This performs the MUXing and deMUXing between the high-speed line interface data operating at the line rate and system data operating at 1/4 or 1/8 the line rate.

On-board PLLs: This is used to align system-side data with the line-side data which is at a slightly higher data bandwidth than the system data because of the addition of overhead due to encoding.

Figure 1 shows the ORLI10G block diagram.

10G Mode

The ORLI10G can operate in one of two data modes: 10G mode or Quad 2.5G mode.

In 10G (or single channel) mode, all 16 LVDS transmit data outputs are assumed to be one data bus with one LVDS clock provided off chip for the data. Likewise, all 16 LVDS receive data inputs are assumed to be one data bus with one LVDS input clock provided for the data.

Transmit Path

In 10G mode, the transmit data from the FPGA logic is passed to the embedded core as a single 128- or 64-bit bus. An off-chip transmit reference clock is divided down in the core by 8 (for 128-bit to 16-bit MUX) or by 4 (for 64-bit to 16-bit MUX). All four transmit clock outputs are therefore synchronized.

ORLI10G Overview (continued)

Receive Path

The 16-bit receive data is deMUXed in the embedded core to a single 128-bit or 64-bit data bus and passed to the FPGA logic. The lowest-order LVDS input clock (rx_clk_in[0]) is used as the receive clock for all 16 data bits (the other three LVDS input clock pairs should be tied low). This clock is divided down in the core by 8 (for 16-bit to 128-bit deMUX) or by 4 (for 16-bit to 64-bit deMUX) and passed to the FPGA logic with the data.

The ORLI10G supports transmit and receive data rates up to 667 Mbits/s. Therefore, the total data rate for this mode is 667 Mbits/s x 16 or 10.672 Gbits/s.

2.5G Mode

In 2.5G (or quad channel) mode, the 16 LVDS transmit data outputs are assumed to be four 4-bit data buses with four LVDS clocks provided off chip for each data bus. Likewise, the 16 LVDS receive data inputs are assumed to be four independent 4-bit data buses with four LVDS asynchronous input clocks provided for each data bus.

Transmit Path

In 2.5G mode, the transmit data from the FPGA logic is passed to the embedded core as four separate 32- or 16-bit buses. A separate clock for each of the four busses is also passed to the core. An off-chip transmit reference clock is divided down in the core by 8 (for each 32 to 8-bit MUX) or by 4 (for each 16 to 4 MUX). This divided down clock is used to resynchronize the output data and clocks. All four transmit clock outputs are therefore synchronized.

Receive Path

Each of the four 4-bit receive data buses are deMUXed in the embedded core to one of four independent 32- or 16-bit data buses and passed to the FPGA logic. The four receive clock inputs are divided down in the core by 8 (for each 4- to 32-bit deMUX) or by 4 (for each 4- to 16-bit deMUX) and each divided clock is passed to the FPGA logic with its associated data bus. All four data paths act as separate data interfaces that are asynchronous to each other.

The ORLI10G supports transmit and receive data rates up to 667 Mbits/s. Therefore, the total data rate each of the quad channels is thus 667 Mbits/s x 4 or 2.5 Gbits/s.

Figure 2 shows a representation of the 10G and 2.5G modes in both transmit and receive directions.

ORLI10G Overview (continued)

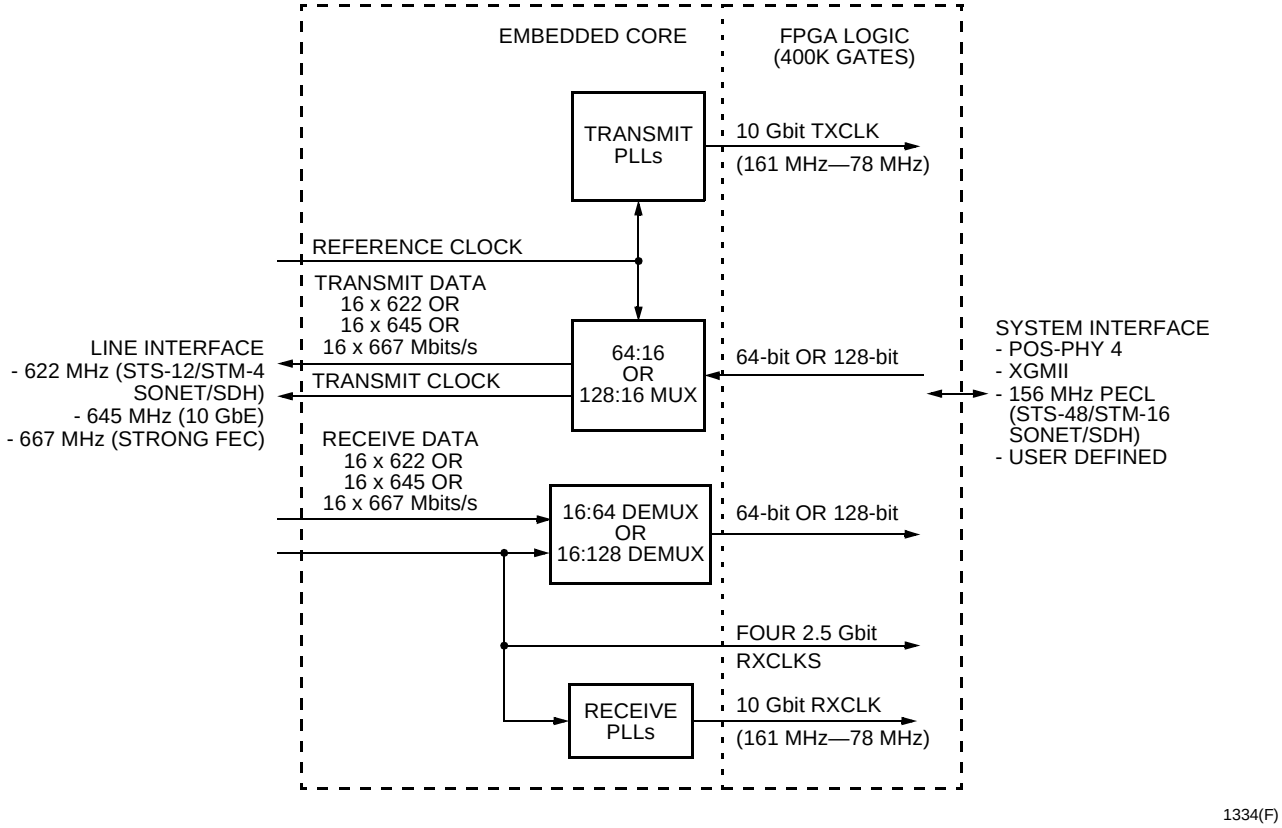


Figure 1. *ORCA* ORLI10G Block Diagram

ORLI10G Overview (continued)

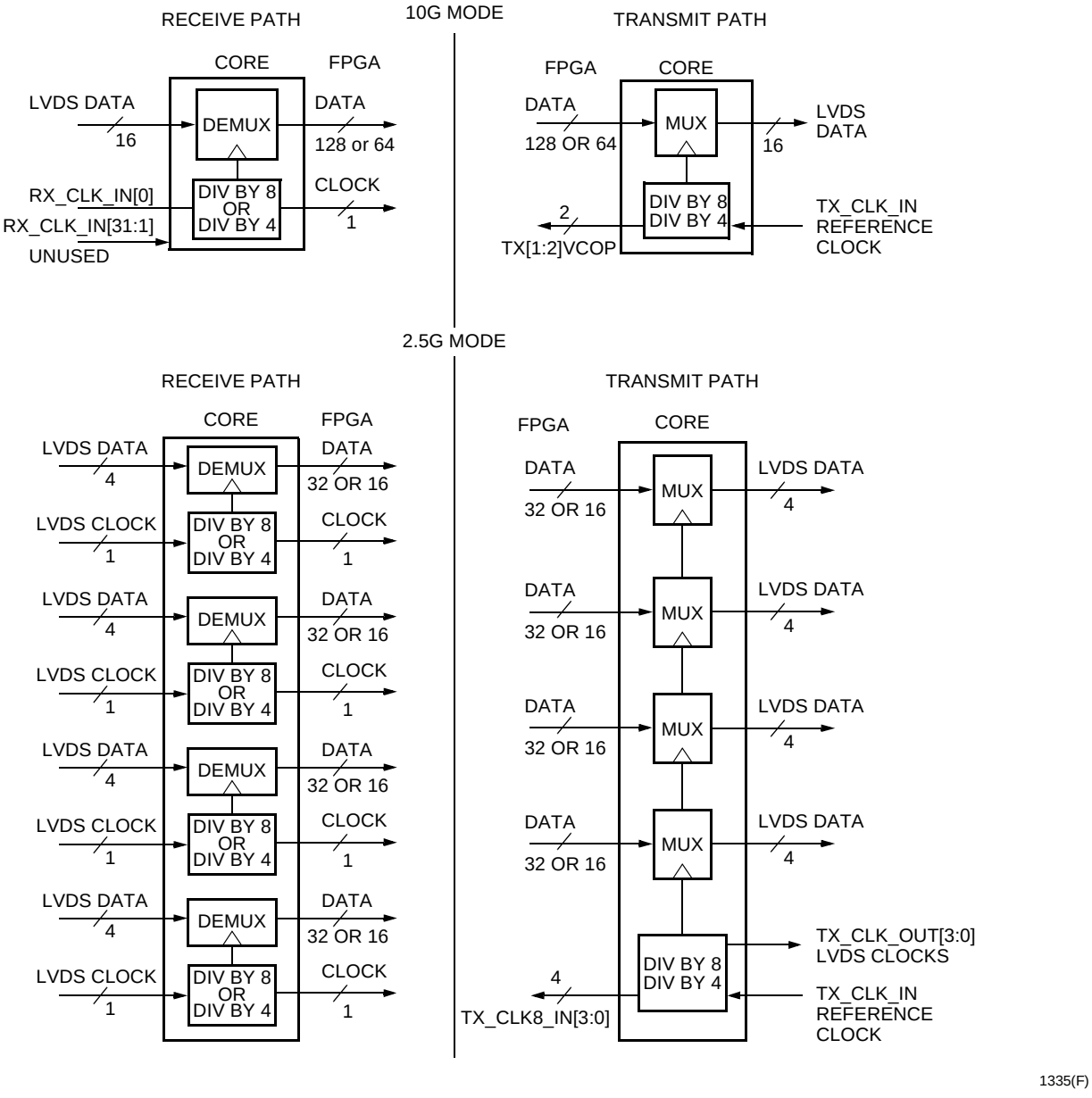


Figure 2. 10G (Single Channel) and 2.5G (Quad Channel) Modes

ORLI10G Overview (continued)

Receive Path

In the receive path, the ORLI10G embedded core can be broken down into three sections: the high-speed line interface, the demultiplexer, and the receive-side onboard PLLs. Note that both transmit and receive PLLs are in addition to the four programmable PLLs (PPLLs) in the FPGA portion of the ORLI10G.

Line Interface

In the receive path, 16-bit data and associated clocks are inputs to the line interface. Typical data rates are expected to range from 622 Mbits/s to 667 Mbits/s for most applications. The 16-bit LVDS input data bus is actually composed of four 4-bit data busses with one clock for each four bit data bus. In the 10G mode, all four input clocks are tied together internal to the device and driven by the lowest-order input clock. In 2.5G mode, the four clocks may be asynchronous to each other. The ORLI10G uses LVDS (low voltage differential signaling) drivers/receivers which are intended to provide point-to-point connection between the ORLI10G and optical transceiver (MUX/deMUX) parts. The LVDS inputs are hot-swap compatible and can connect to other vendor's LVDS I/O buffers. The LVDS inputs are terminated with a 100 Ω resistor to improve performance.

DeMUX

The demultiplexer takes the high-speed line data and clocks and converts the data and clock to rates appropriate for transfer to the FPGA logic. The demultiplexer supports two modes of operation:

- Divide-by-8

10G (or single channel): The demultiplexer converts the incoming 16 bits of data at 622 Mbits/s to 667 Mbits/s to 128 bits at 78 Mbits/s to 83 Mbits/s. The incoming clocks are divided by 8.

2.5G (or quad channel): The demultiplexer converts the incoming four bits of data at 622 Mbits/s to 667 Mbits/s to 32 bits at 78 Mbits/s to 83 Mbits/s. The associated clock is also divided by 8. This is repeated four times with each 4-bit data/clock group assumed to be asynchronous to the others.

- Divide-by-4

10G (or single channel): The demultiplexer converts the incoming 16 bits of data at 622 Mbits/s to 667 Mbits/s to 64 bits at 156 Mbits/s to 166 Mbits/s. The incoming clocks are divided by 4.

2.5G (or quad channel): The demultiplexer converts the incoming four bits of data at 622 Mbits/s to 667 Mbits/s to 16 bits at 156 Mbits/s to 166 Mbits/s. The associated clock is also divided by 4. This is repeated four times with each 4-bit data/clock group assumed to be asynchronous to the others.

Onboard Receive PLLs

The function of the onboard PLLs is to align the system data with the line data which will be at a slightly higher rate owing to the addition of the overhead bits. There are two PLLs on the receive path. The input to the first PLL, RX1_PLL (see Figure 3), is the divided down lowest-order clock from the demultiplexer. The RX1_PLL generates a clock with a user-defined frequency ratio of M/N to the divided clock. This clock would generally be used to compensate for different data rates due to overhead bits. M and N can independently be set from 1 to 40.

The RX2_PLL also takes its input from the divided down clock and is used to provide a balanced divided clock across the FPGA-embedded core interface.

Both PLLs have delay loops which compensate for routing delays to the embedded core/FPGA logic interface for minimum clock skew.

In addition, the user can specify an additional skew on each clock in increments of 1/8 the clock period.

The selection of the deMUX width (and corresponding clock division value), the RX1_PLL M and N values, and the additional skew for RX1_PLL and RX2_PLL are specified by the user in a GUI interface provided in the ORLI10G design kit.

A detailed block diagram of the receive path in shown in Figure 3.

ORLI10G Overview (continued)

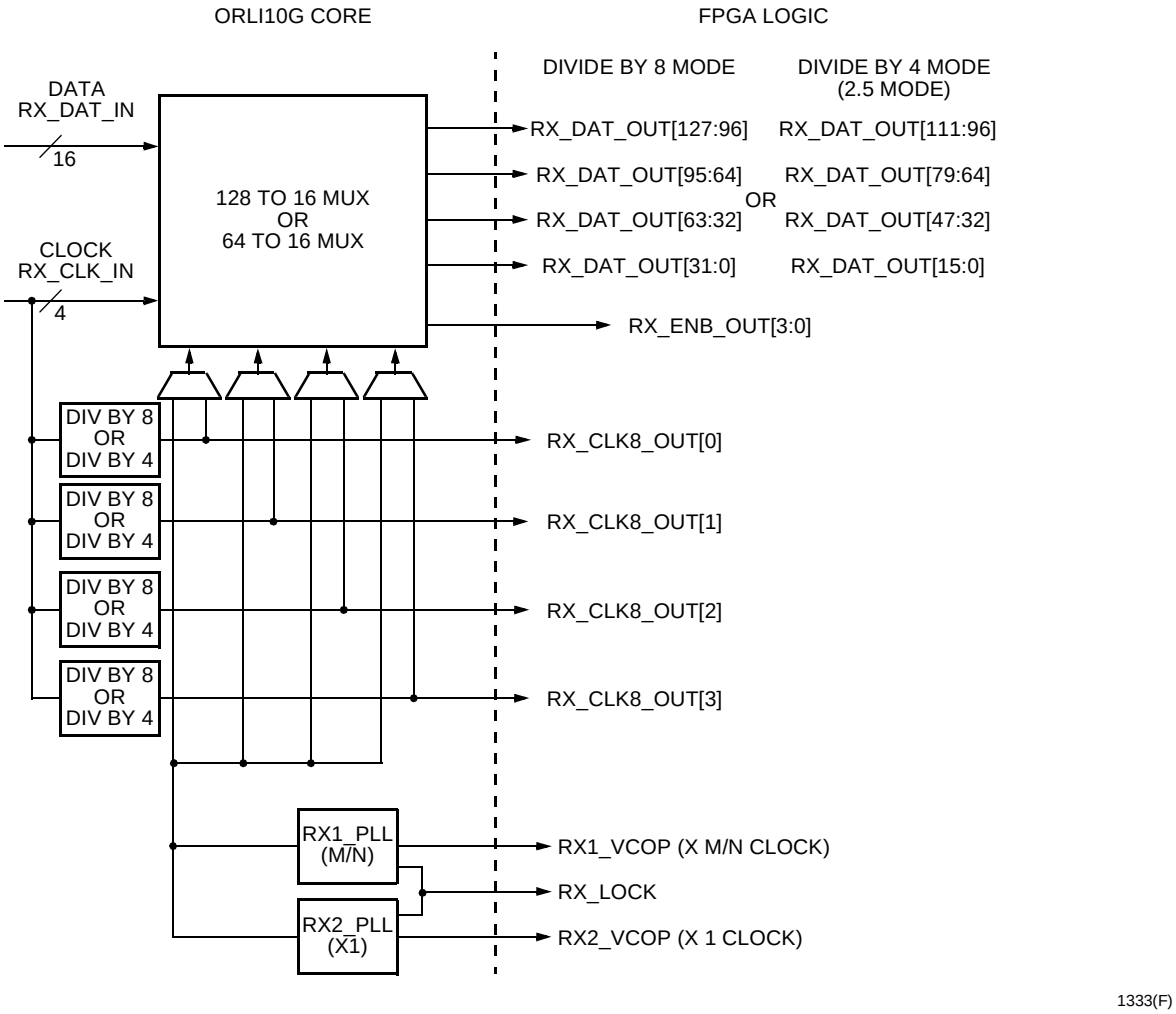


Figure 3. ORLI10G Embedded Core Receive Path Diagram

ORLI10G Overview (continued)

Transmit Path

In the transmit path, the ORLI10G embedded core can be broken down into three sections: the multiplexer, the transmit side onboard PLLs, and the high-speed line interface. Note that both transmit and receive PLLs are in addition to the four programmable PLLs (PPLLs) in the FPGA portion of the ORLI10G.

MUX

The multiplexer takes data from the FPGA logic and multiplexes the data to rates for transfer by the high-speed line interface. The multiplexer supports two modes of operation:

- Multiplex-by-8

The multiplexer converts the incoming 128 bits of data at 78 Mbits/s to 83 Mbits/s to 16 bits at 622 Mbits/s to 667 Mbits/s. The incoming transmit reference clock is divided by 8.

- Multiplex-by-4

10G (or single channel): The multiplexer converts the incoming 64 bits of data at 156 Mbits/s to 166 Mbits/s to 16 bits at 622 Mbits to 667 Mbits/s. The transmit reference clock is divided by 4.

Onboard Transmit PLLs

The function of the onboard PLLs is to align the system data with the line data which will be at a slightly higher rate owing to the addition of the overhead bits. There are two PLLs on the transmit path. The input to the first PLL, TX1_PLL (see Figure 4), is the divided down transmit reference clock from the multiplexer. The TX1_PLL generates a clock with a user-defined frequency ratio of M/N to the divided clock. This clock would generally be used to compensate for different data rates due to overhead bits. M and N can independently be set from 1 to 40.

The TX2_PLL also takes its input reference from the divided down reference clock and is used to provide a balanced divided clock across the FPGA-embedded core interface.

Both PLLs have delay loops which compensate for routing delays to the embedded core/FPGA logic interface for minimum clock skew.

In addition, the user can specify an additional skew on each clock in increments of 1/8 the clock period.

The selection of the MUX width (and corresponding clock division value), the TX1_PLL M and N values, and the additional skew for TX1_PLL and TX2_PLL are specified by the user in a GUI interface provided in the ORLI10G deisng kit.

A detailed block diagram of the transmit path in shown in Figure 4.

Line Interface

In the transmit path, 16-bit data and associated clocks are outputs from the line interface. Typical data rates are expected to range from 622 Mbits/s to 667 Mbits/s for most applications. The 16-bit LVDS output data bus is actually composed of four 4-bit data buses with one clock for each 4-bit data bus. On the transmit side, these clocks will all be synchronized. The ORLI10G uses LVDS (low-voltage differential signaling) drivers/receivers which are intended to provide point-to-point connection between the ORLI10G and optical transceiver (MUX/deMUX) parts. The LVDS drivers are hot-swap compatible and can connect to other vendor's LVDS I/O buffers. The LVDS drivers are terminated with a 100 Ω resistor to improve performance.

ORLI10G Overview (continued)

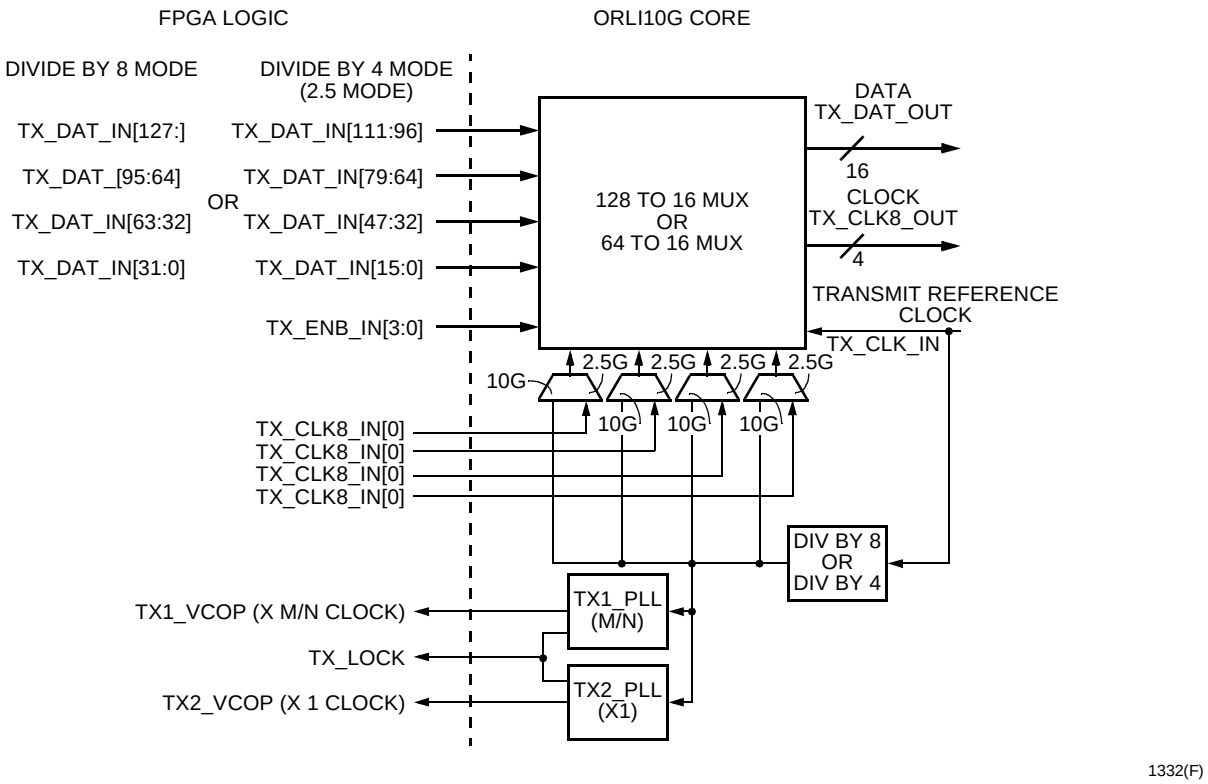


Figure 4. ORLI10G Embedded Core Transmit Path Diagram

ORLI10G Demultiplexer Detail

The demultiplexer module converts the incoming 16 bits of data at 622 MHz/666 MHz into 128 bits of data at 78 MHz/83 MHz. It has been implemented in two stages: the first stage converts each incoming bit into a byte stream and the second stage bit interleaves these bytes into 128 bits depending upon the mode of operation. The low-speed clocks are generated by this block. These clocks are then driven back to this block from the low speed clock tree network. Functionally, the demultiplexer architecture consists of three blocks; the serial to parallel conversion, the counters, and the interleaving.

The first stage of the line interface module (demultiplexer) converts each incoming bit of data into a byte stream on a divided by 8 clock. The data is first registered on the rising edge of the clock input. The clock dividers also runs parallel to data shift (serial to parallel), on the rising edge of the input clock. An enable is created when a complete byte is taken in. This enable signal is used to register the serial-to-parallel converted data at the high-speed input clock. This ensures that the data can be safely transferred to the low-speed clock. This data is then transferred to the divided clock allowing a timing margin of approximately half the divided clock period.

The high-speed demultiplexer converts the incoming data as blocks of bytes. The byte boundaries of incoming data are unknown and are irrelevant to this module. This data is then interleaved to the 128/32 bits of output data depending on the mode of operation (10G/2.5G). In 10G mode, the output data is assigned the retimed 128 bits of data from the first stage of line interface registered at the input clock [0]. In 2.5G mode, the output data is assigned four concatenated 32 bits of data from the first stage of line interface registered at input clocks [0 to 3]. The interleaving is done at bit level because the serial-to-parallel converter operates on bits of incoming data. In 10G mode, it is assumed that all the incoming 16 bits of data are synchronized to the input clock [0]. This block also generates the clock enables used by the output line interface (multiplexer) module for registering the data on the high-speed clock. These enables along with the enables from other clocks are selected through the high-speed clock MUX for the output line interface block.

ORLI10G Demultiplexer Detail (continued)

Figure 5 shows the valid data output bits from the demultiplexer in each of the four modes (divide-by-8, 10G and 2.5G modes, and divide-by-4, 10G and 2.5G modes). Figure 6—Figure 9 show the demultiplexer input data and clock waveforms and output clock, enable, and data waveforms for all four modes.

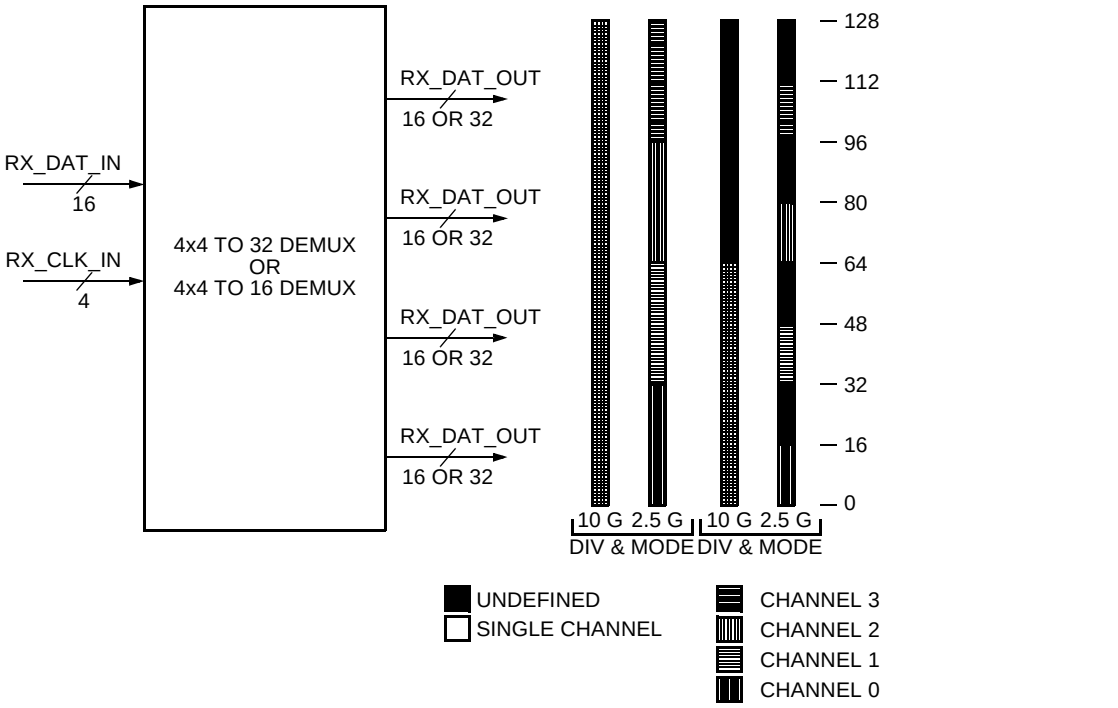


Figure 5. Demultiplexer Output Data Structure

ORLI10G Demultiplexer Detail (continued)

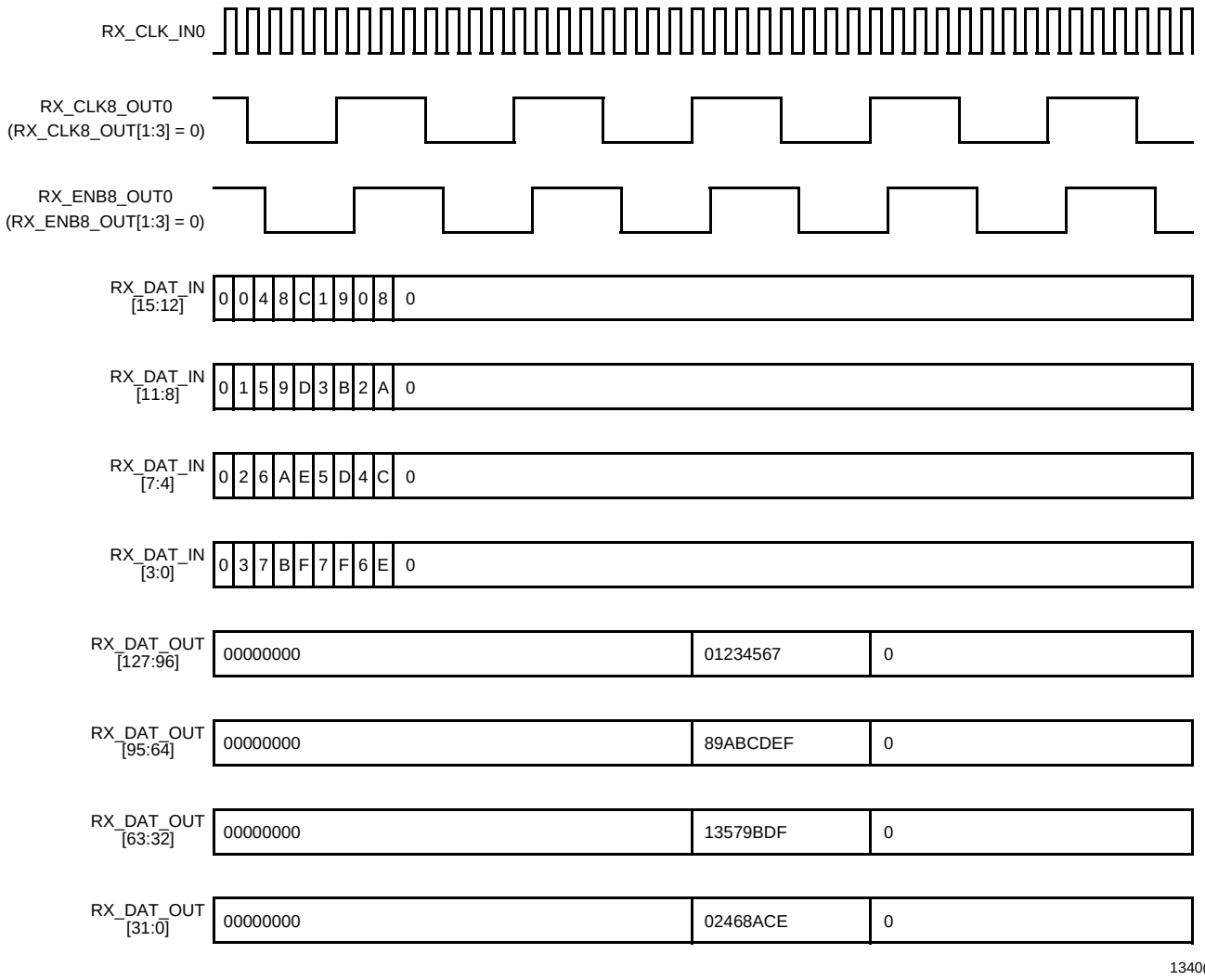


Figure 6. Demultiplexer Serial-to-Parallel Conversion—Divide by 8, 10G Mode

ORLI10G Demultiplexer Detail (continued)

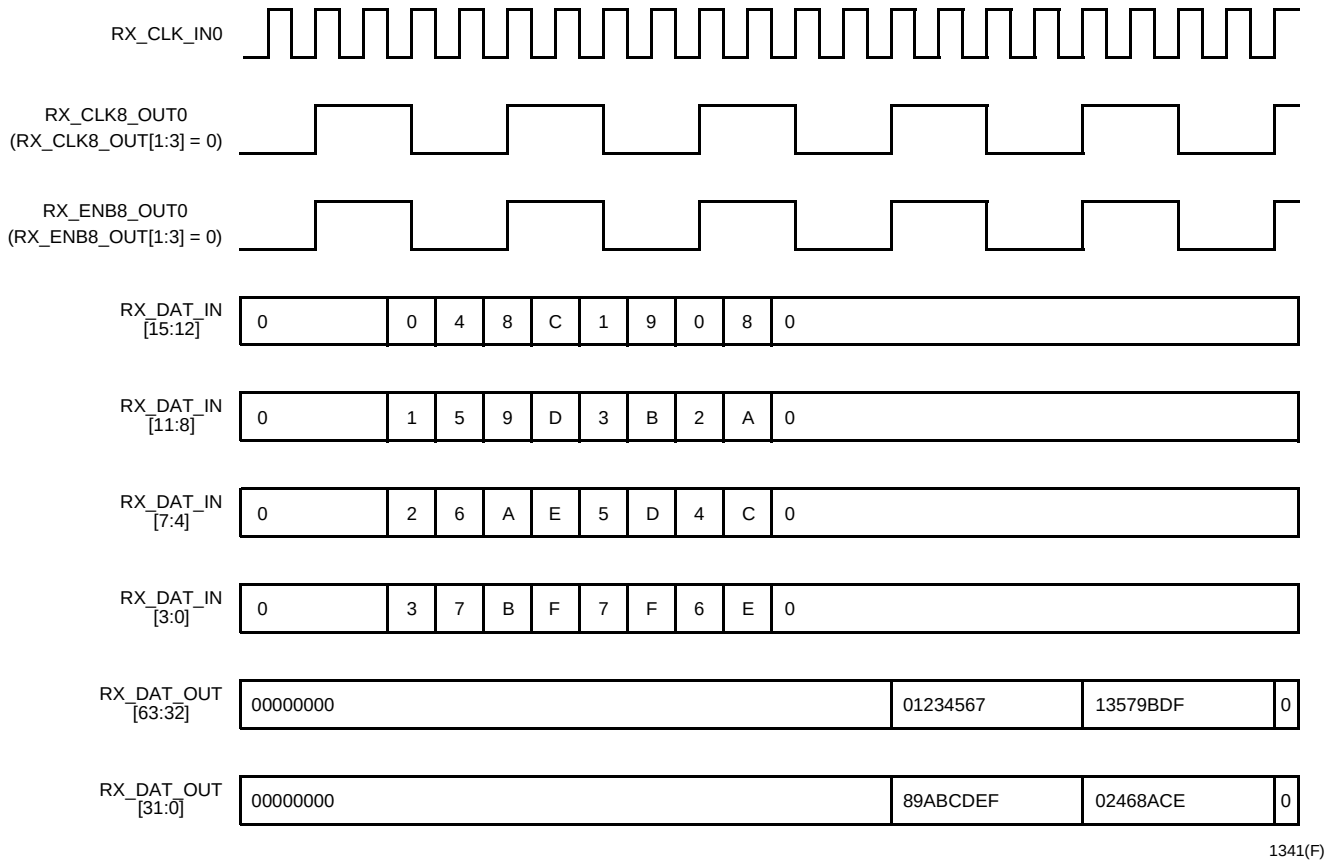


Figure 7. Demultiplexer Serial-to-Parallel Conversion—Divide by 4, 10G mode

ORLI10G Demultiplexer Detail (continued)

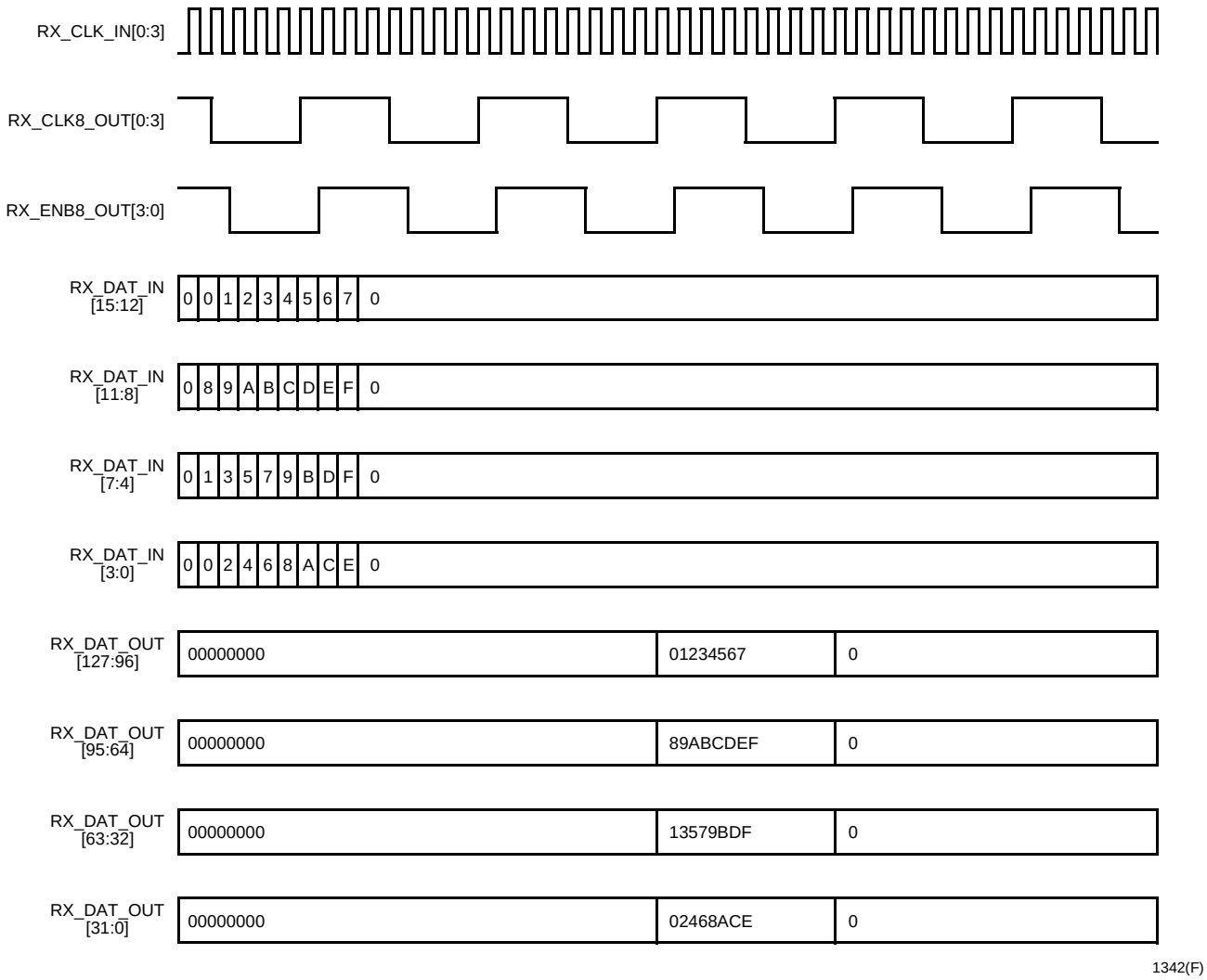


Figure 8. Demultiplexer Serial-to-Parallel Conversion—Divide by 8, 2.5G Mode

ORLI10G Demultiplexer Detail (continued)

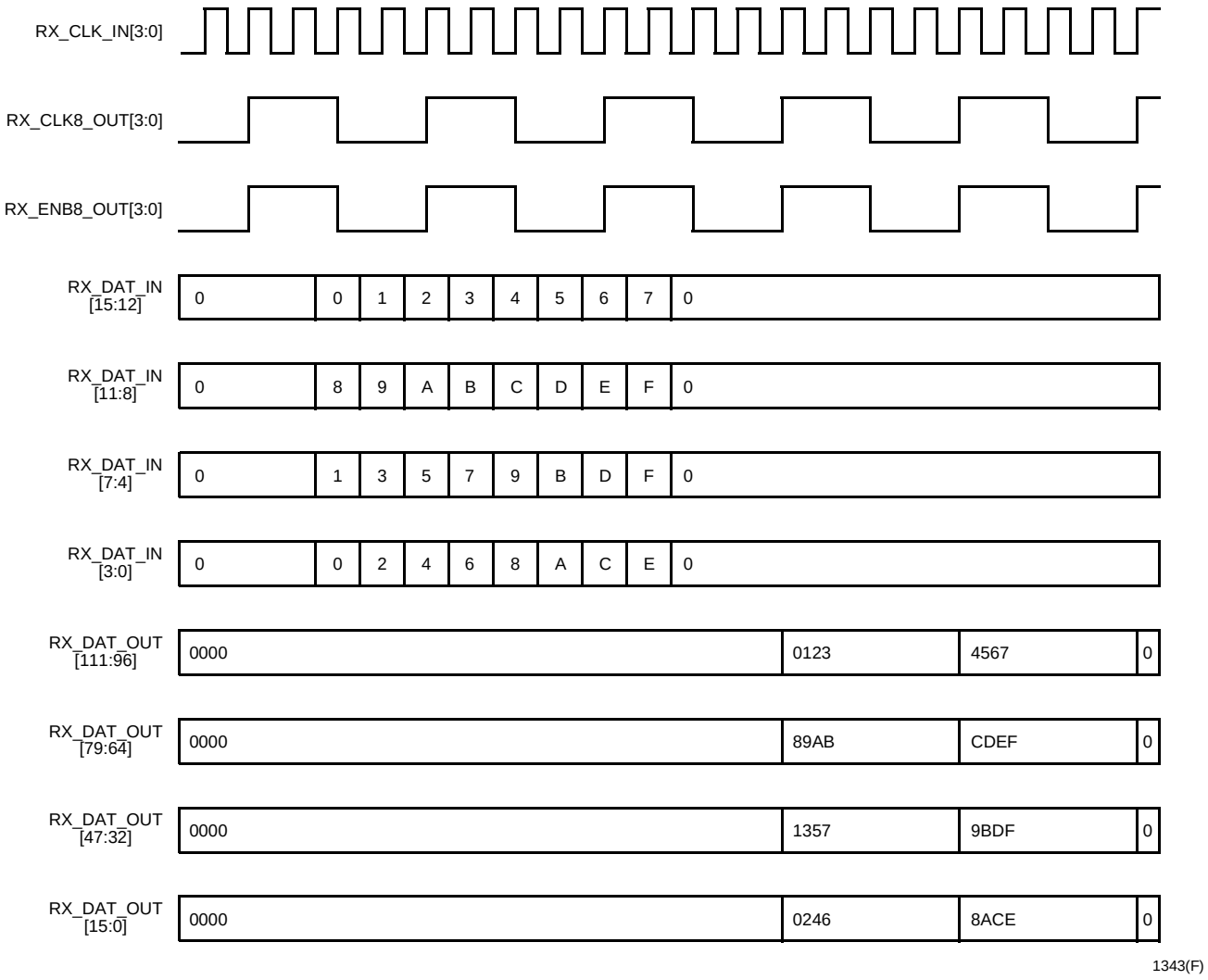


Figure 9. Demultiplexer Serial-to-Parallel Conversion—Divide by 4, 2.5G mode

ORLI10G Multiplexer Detail

The multiplexer module converts the incoming 128 bits of data at 78 MHz/83 MHz or 64 bits of data at 156 MHz/166 MHz into 16 bits of data at 622 MHz/666 MHz. It has been implemented as two stages. The first stage deinterleaves each incoming byte into a different byte stream that can be serially output on the output data pins. The second stage outputs these bytes into 16 bits or four groups of 4 bits depending upon the mode of operation. Functionally, the multiplexer architecture consists of three blocks: the parallel-to-serial conversion, the counters, and the deinterleaving.

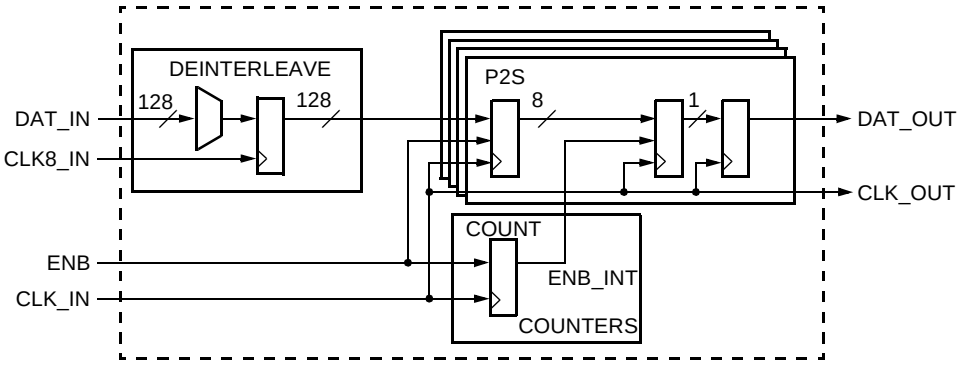
For 2.5G divide-by-8 mode, the first stage of the line interface module deinterleaves each incoming byte of data into a different byte stream on the 78 MHz/83 MHz clock. This data is first registered on the rising edge of the 622 MHz/666 MHz clock input. The data is registered at a time when it is safe to do so; in this case, it is nearer to the falling edge of the 78 MHz/83 MHz clock. The enable inputs are used to transfer data from the low-speed clock to the high-speed clock as well as synchronizing the counters of parallel-to-serial conversion which are running at the high-speed clock. The block diagram is shown in Figure 10.

For 2.5G divide-by-4 mode, the first stage of the line interface module deinterleaves each incoming byte of data into a different byte stream on the 156 MHz/166 MHz clock. This data is first registered on the rising edge of the 622 MHz/666 MHz clock input. The data is registered at a time when it is safe to do so; in this case, it is nearer to the falling edge of the 156 MHz/166 MHz clock. The enable inputs are used to transfer data from the low-speed clock to the high-speed clock as well as synchronizing the counters of parallel-to-serial conversion which are running at the high-speed clock. The block diagram is also shown in Figure 10.

In 2.5G modes, the enable inputs are assumed to be four clock cycles wide and are shortened internally. They have to be synchronous to their corresponding clock. In single channel operation, the four groups of 4 bits must have relationship to the slice zero clock. In single-channel mode, all the enable inputs are to be identical (generated from the slice zero clock).

In 10G mode the enable signal in generated internally from the transmit reference clock.

Figure 11 shows the valid data input bits to the multiplexer in each of the four modes (divide-by-8, 10G and 2.5G modes, and divide-by-4, 10G and 2.5G modes). Figure 12—Figure 15 show the multiplexer input transmit reference clock, data, enable, and clock waveforms and output clock and data waveforms for all four modes.



1336(F)

Figure 10. Multiplexer Interface

ORLI10G Multiplexer Detail (continued)

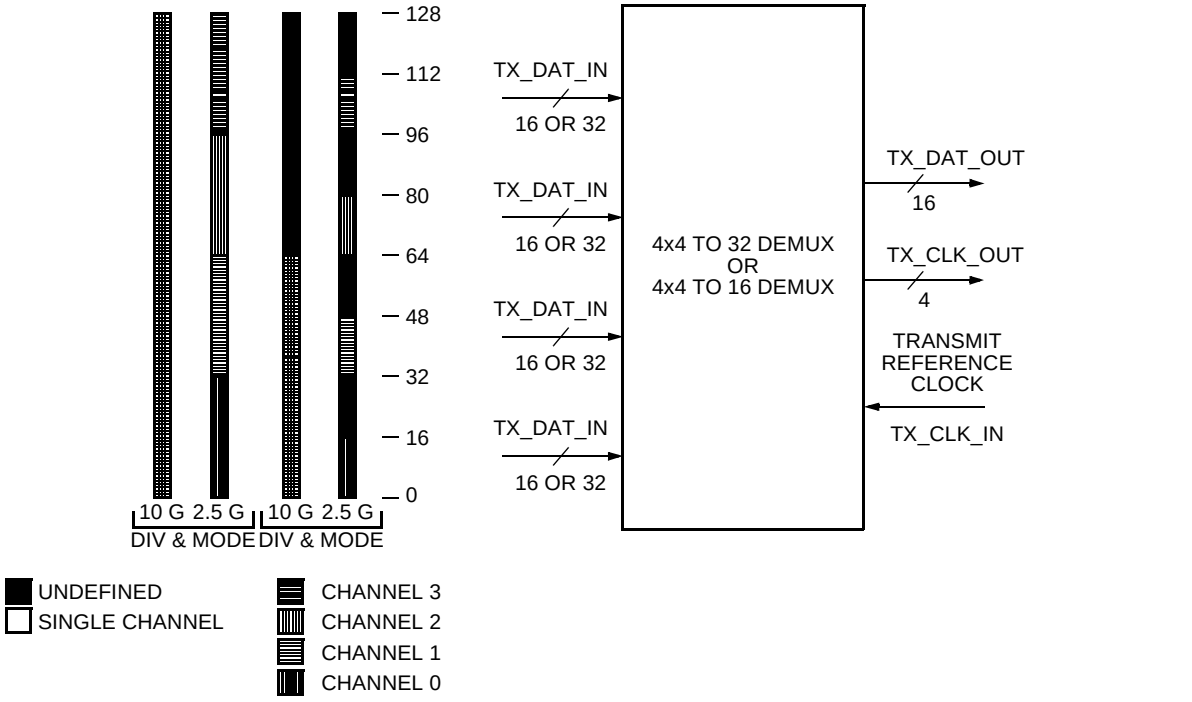


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Figure 11. Multiplexer Input Data Structure

ORLI10G Multiplexer Detail (continued)

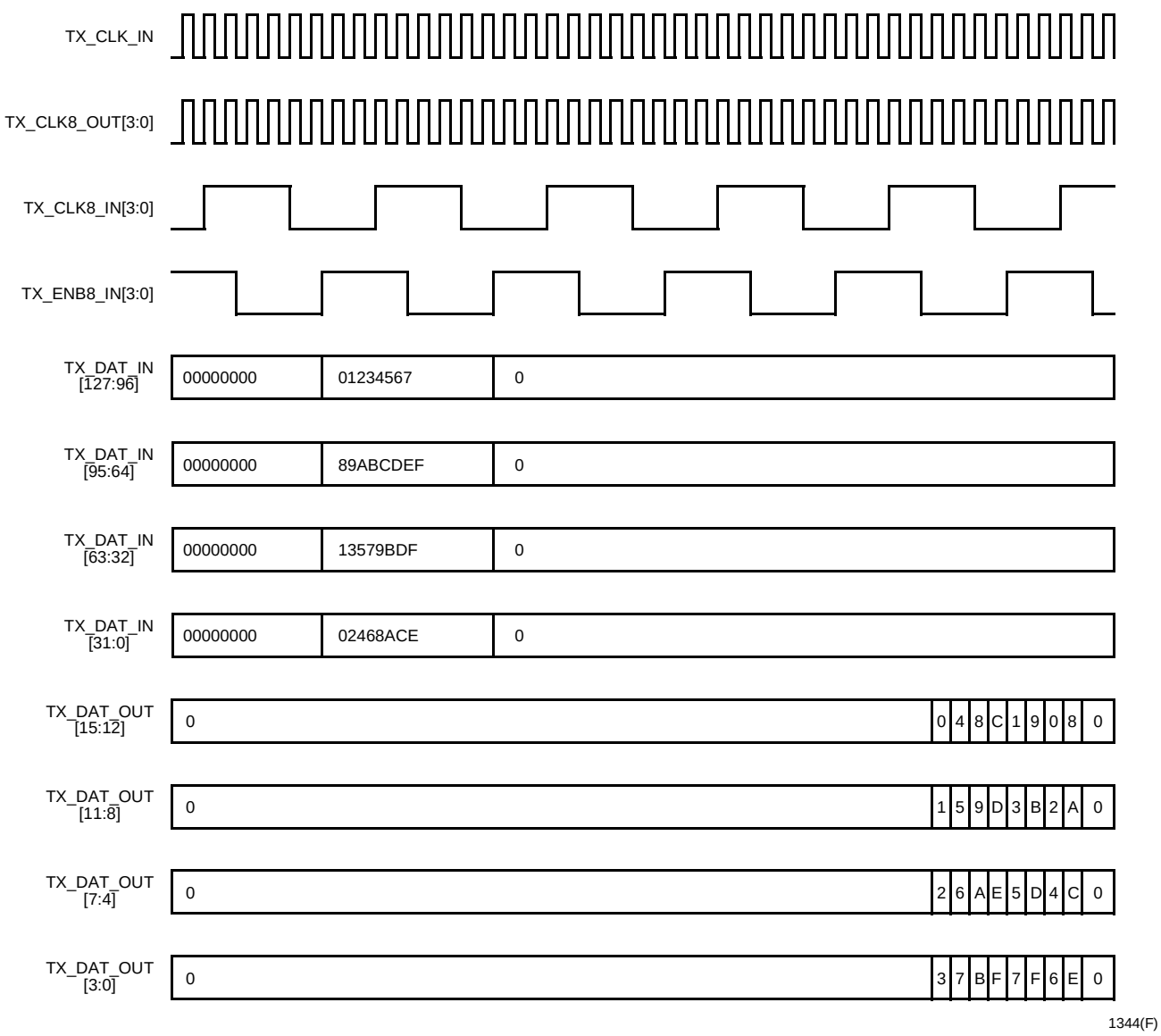


Figure 12. Multiplexer Parallel-to-Serial Conversion—Divide by 8, 10G Mode

ORLI10G Multiplexer Detail (continued)

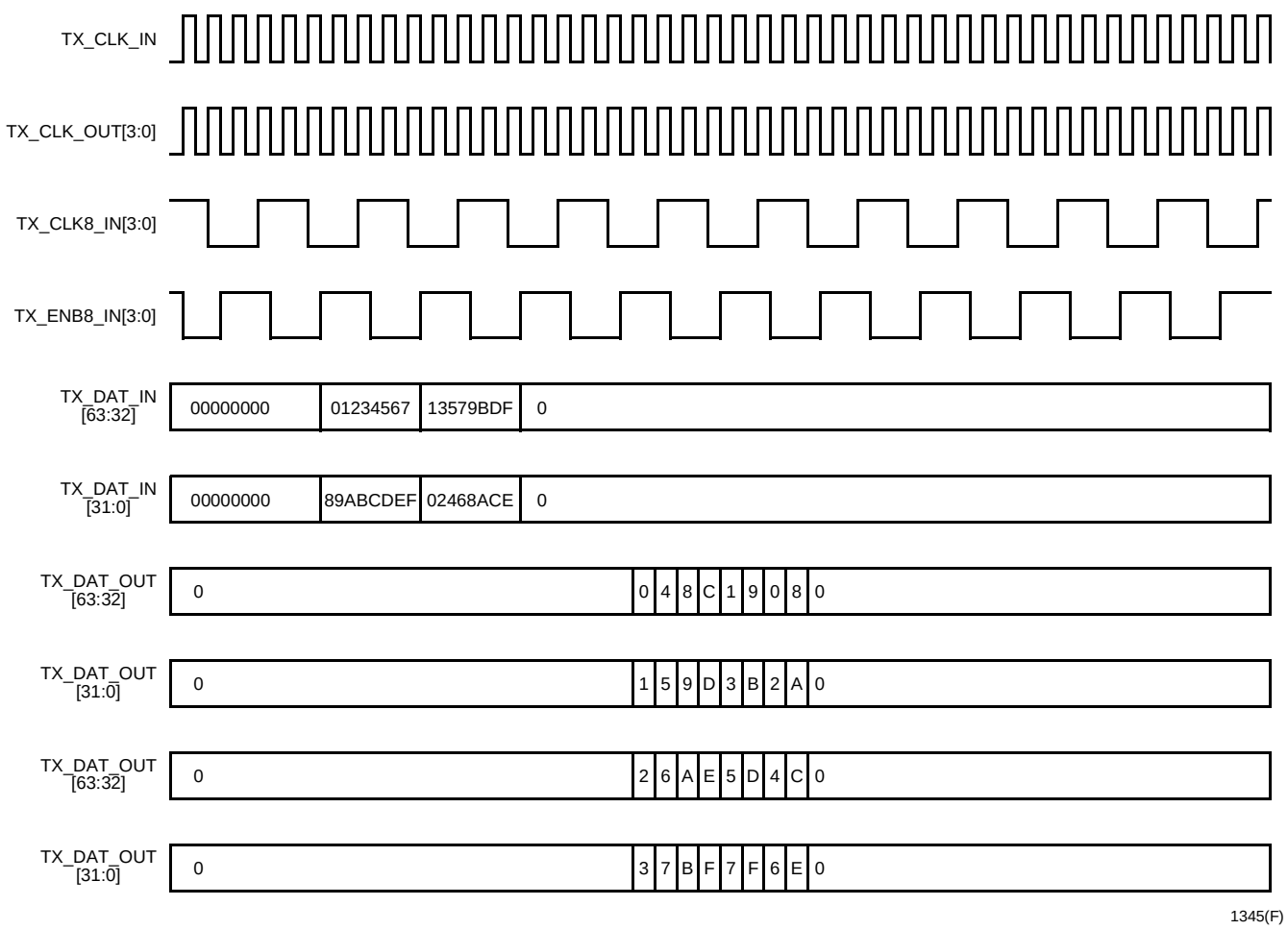


Figure 13. Multiplexer Parallel-to-Serial Conversion—Divide by 4, 10G Mode

ORLI10G Multiplexer Detail (continued)

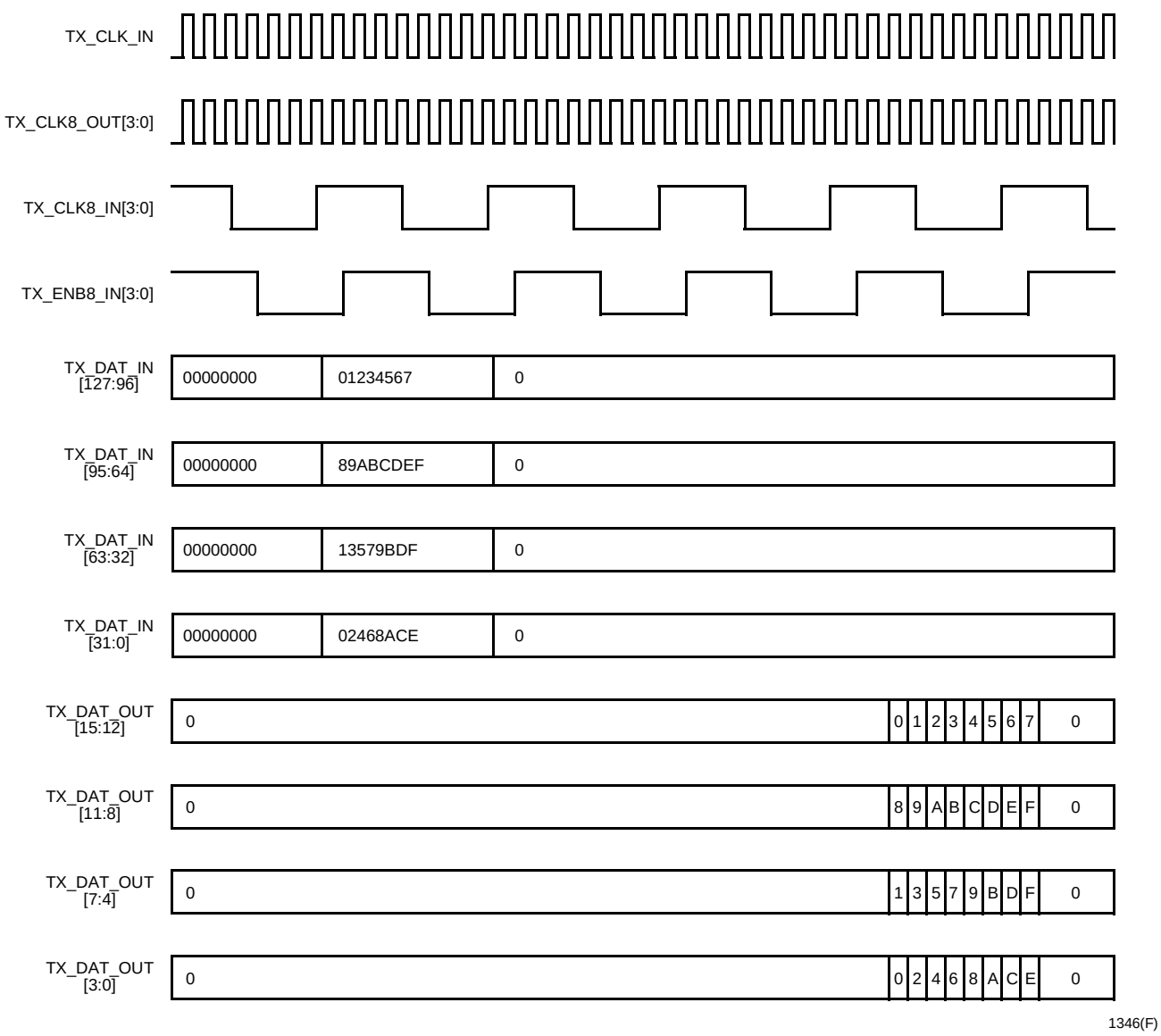


Figure 14. Multiplexer Parallel-to-Serial Conversion—Divide by 8, 2.5G Mode

ORLI10G Multiplexer Detail (continued)

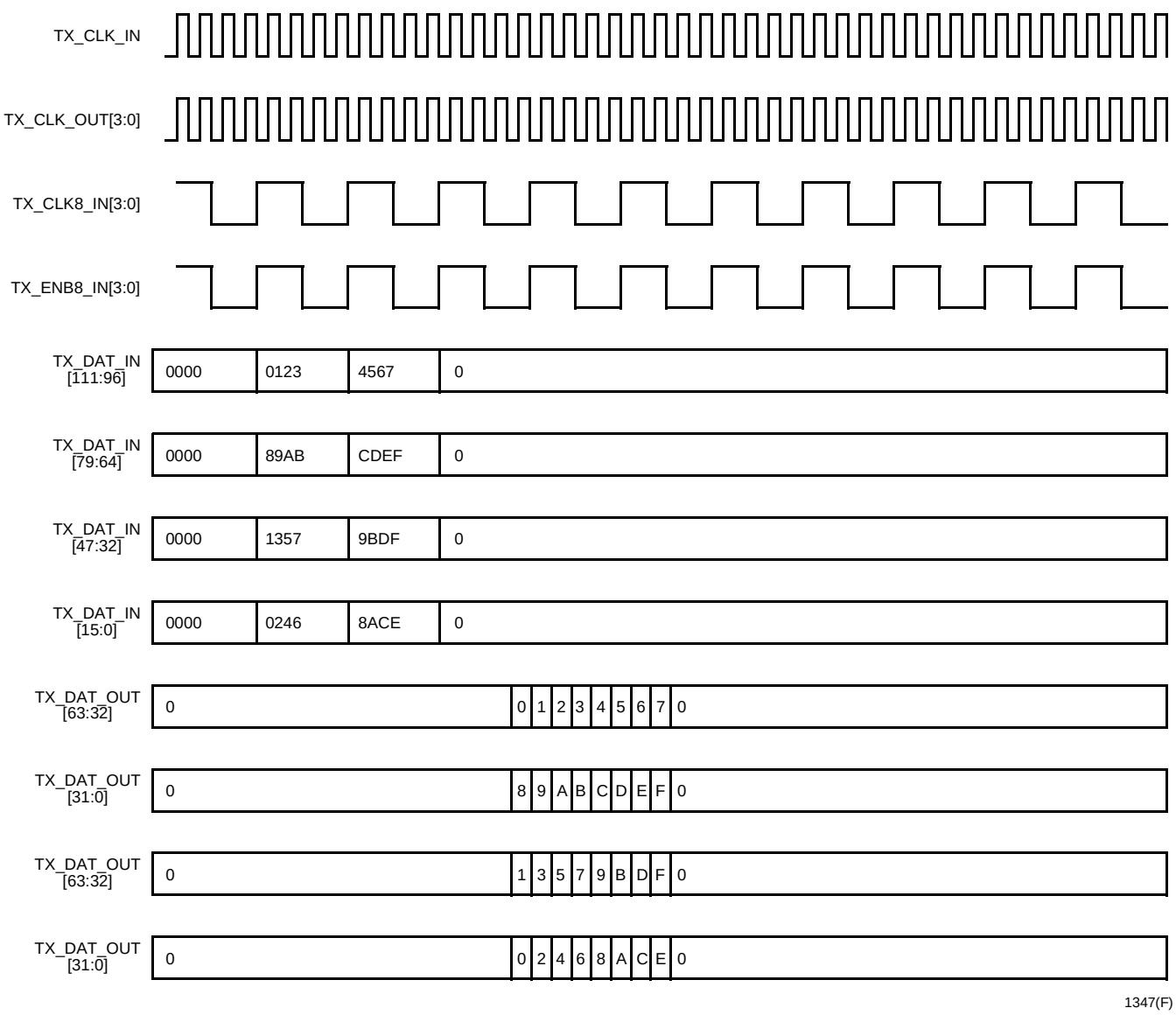


Figure 15. Multiplexer Parallel-to-Serial Conversion—Divide by 4, 2.5G Mode

ORLI10G Embedded PLLs

The ORLI10G embedded (transmit and receive) PLLs are based on the 4E series FPGA high-speed programmable PLL. The 4E PLL consists of a phase/frequency detector (PFD), a charge pump/filter, a multitap voltage controlled oscillator (VCO), a duty cycle synthesis circuitry, a power regulator, two programmable dividers, phase shift selector multiplexers, a lock signal generator, and a current DAC. A block diagram of the programmable PLL is shown in Figure 16. The receive path RX1_PLL and transmit path TX1_PLL, which can be programmed to create a N/M frequency clock, are based on this design.

The receive path RX2_PLL and transmit path TX2_PLL create a X1 clock. This is essentially the same PLL without the M and N divider.

The clock feedback loops for each PLL have been routed in the core so as to compensate for the routing delays to the FPGA logic interface. In this way, the clock skew at the embedded core/FPGA logic boundary is zero for the receive and transmit PLLs.

All PLLs include a phase shift selector which allows phase shift adjustments of each clock in increments of 1/8 the period of the clock.

All functions of the embedded core PLLs are user controlled through a GUI provided with the ORLI10G Design Kit software.

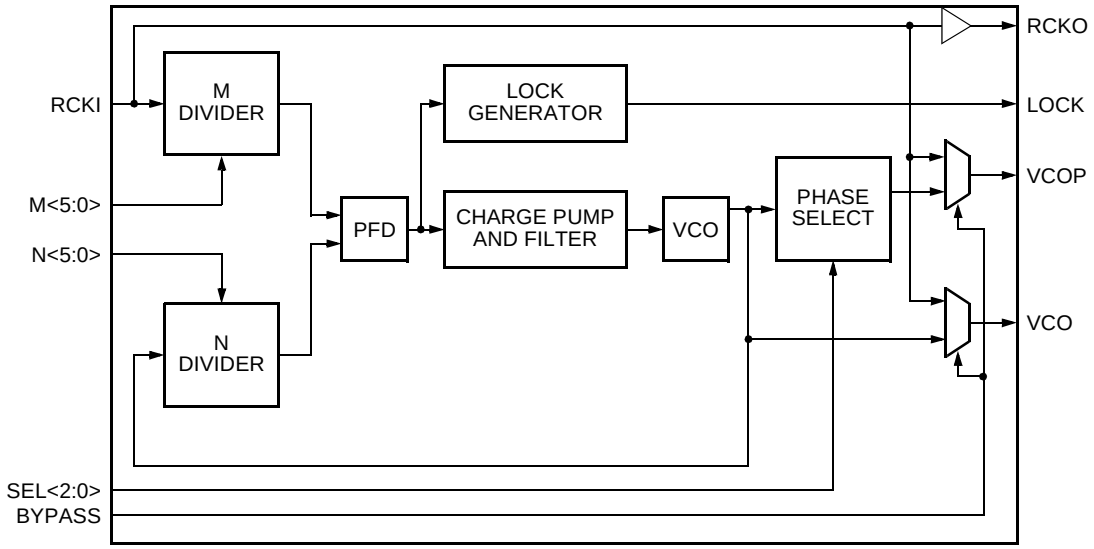


Figure 16. ORLI10G Programmable PLL Block Diagram

ORLI10G Embedded Programmable PLLs Specifications

Table 2. Programmable PLL Specifications

Parameters	Min	Nom	Max	Unit
V_{DD} 1.5	1.425	1.5	1.575	V
V_{DD} 3.3	3.0	3.3	3.6	V
Operating Temperature	–40	25	125	°C
Input Clock Voltage	1.425	1.5	1.575	V
Output Clock Voltage	1.425	1.5	1.575	V
Input Clock Frequency	60	—	667	MHz
Output Clock Frequency	60	—	667	MHz
Output Duty Cycle	45	50	55	%
dc On Power Consumption	—	50	—	mW
Total On Current (dc)	—	14.0	—	mA
Total Off Current (dc)	—	30.0	—	pA
Cycle to Cycle Jitter(p-p)	—	< 0.02	—	UIpp
Lock Time	—	< 50	—	µs
Frequency Multiplication	1—40X			—
Frequency Division	1—40X			—
Phase Shift Between VCOP and VCO	0, 45, 90, 135, 180, 225, 270, 315			degree

LI Circuit Specifications

Power Supply Decoupling LC Circuit

The 622 MHz—667 MHz LI macro contains both analog and digital circuitry. The data recovery function, for example, is implemented as primarily a digital function, but it relies on a conventional analog phase-locked loop to provide its 622 MHz—667 MHz reference frequency. The internal analog phase-locked loop contains a voltage-controlled oscillator. This circuit will be sensitive to digital noise generated from the rapid switching transients associated with internal logic gates and parasitic inductive elements. Generated noise that contains frequency components beyond the bandwidth of the internal phase-locked loop (about 3 MHz) will not be attenuated by the phase-locked loop and will impact bit error rate directly. Thus, separate power supply pins are provided for these critical analog circuit elements.

Additional power supply filtering in the form of a LC pi filter section will be used between the power supply source and these device pins as shown in Figure 17. The corner frequency of the LC filter is chosen based on the power supply switching frequency, which is between 100 kHz and 300 kHz in most applications.

Capacitors C1 and C2 are large electrolytic capacitors to provide the basic cutoff frequency of the LC filter. For example, the cutoff frequency of the combination of these elements might fall between 5 kHz and 50 kHz. Capacitor C3 is a smaller ceramic capacitor designed to provide a low-impedance path for a wide range of high-frequency signals at the analog power supply pins of the device. The physical location of capacitor C3 must be as close to the device lead as possible. Multiple instances of capacitors C3 can be used if necessary. The recommended filter for the HSI macro is shown below: L = 4.7 µH, RL = 1 Ω, C1 = 0.01 µF, C2 = 0.01 µF, C3 = 4.7 µF.

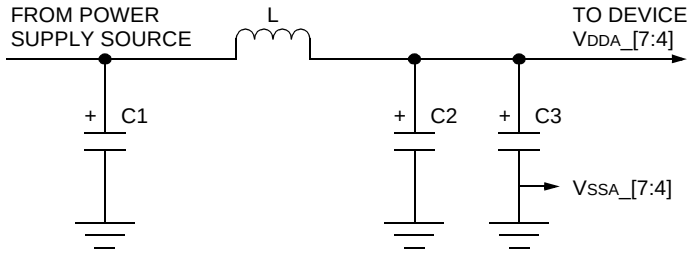


Figure 17. Sample Power Supply Filter Network for Analog LI Power Supply Pins

XGMII *ORCA* 4E Receive Analysis

XGMII Considerations

The stringent 10 Gbit media independent interface specifications from the *IEEE* 802.3ae standards are met in the FPGA side of the ORLI10G device. Figure 18 and Table 3 show a simplified block diagram for this interface and the receive voltage levels for the HSTL inputs to the ORLI10G device.

The ORLI10G device meets the 480 ps input setup time and 480 ps input hold time requirements for the XGMII receiver inputs into the FPGA side of the FPSC with the embedded IO DDR cells and the embedded PLLs on the FPGA side of the FPSC. The PLLs are not used on input due to this being a forward clocked interface. The ORLI10G meets the clock-to-out specification on the XGMII DDR outputs by using the output shift register to produce a nonduty cycle dependent output. The output clock is then centered around this data eye using internal PLLs.

There are two considerations to note about the pinout location of the XGMII input clocks.

1. The XGMII input clocks must be located at the C pad of the programmable I/O Cells (PICs). In the pinout tables, the pads are labelled on a pin-by-pin basis. For example, a pin whose pad is referenced as PL1C can be used as an XGMII input clock, but pins referenced as PL1A, PL1B, or PL1D cannot be used as an XGMII input clock.
2. The XGMII input data pins can be no further then six PICs away from the XGMII input clock pin. This means that in the 416 PBGA package, the clock needs to be driven on two pins to be able to clock in the 32-bit XGMII input data bus.

The only considerations to note about the XGMII output transmit clock is that it needs to be phase-locked with an embedded PLL in the FPGA side of the FPSC.

Due to the strict pinout locations mentioned above, when implementing a XGMII interface, the microprocessor interface (MPI) will not be available in the 416 PBGA and 680 PBGA packages.

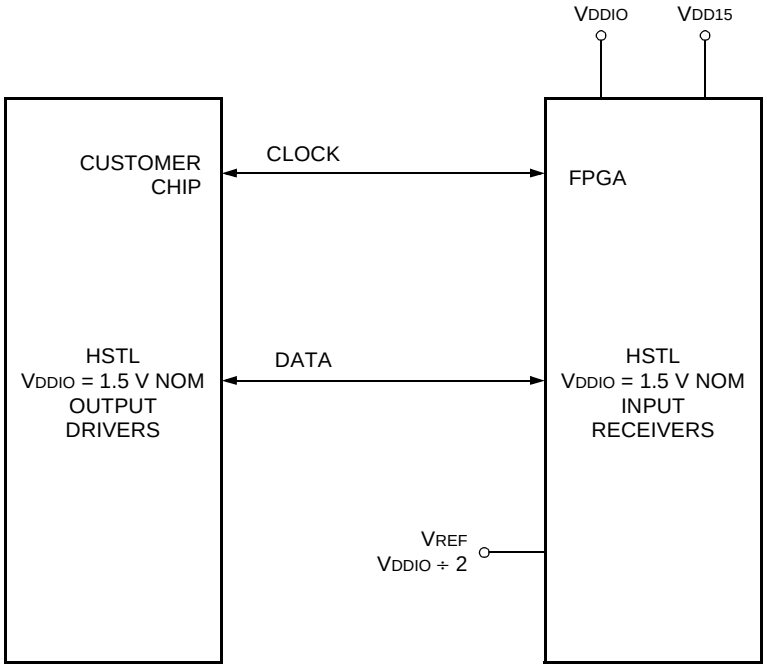


Figure 18. Simplified XGMII Block Diagram

XGMII *ORCA* 4E Receive Analysis (continued)

Table 3. Assumed Inputs to FPGA

Inputs	Low	Nom	High
V_{DDIO}	1.4 V	1.5 V	1.6 V
V_{IH} (min level)	0.88 V	0.95 V	1.10 V
V_{REF}	0.68 V	0.75 V	0.90 V
V_{IL} (max level)	0.48 V	0.55 V	0.70 V

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Power Supply Voltage with Respect to Ground	$V_{DD}3$	—	≤4.2	V
	$V_{DD}15$	—	2	V
Input Signal with Respect to Ground	—	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Signal Applied to High-impedance Output	—	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Maximum Package Body Temperature	—	—	220	°C

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage with Respect to Ground	$V_{DD}3$	2.7	3.6	V
	$V_{DD}15$	1.4	1.6	V
Input Voltages	V_{IN}	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	–40	125	°C

Embedded Core LVDS I/O

Table 6. Driver dc Data*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High, V_{OA} or V_{OB}	V_{OH}	R_{LOAD} = 100 Ω ± 1%	—	—	1.475†	V
Output Voltage Low, V_{OA} or V_{OB}	V_{OL}	R_{LOAD} = 100 Ω ± 1%	0.925†	—	—	V
Output Differential Voltage	$\lvert V_{OD} \rvert$	R_{LOAD} = 100 Ω ± 1%	0.25	—	0.45†	V
Output Offset Voltage	V_{OS}	R_{LOAD} = 100 Ω ± 1%	1.125*	—	1.275†	V
Output Impedance, Differential	R_O	V_{CM} = 1.0 V and 1.4 V	80	100	120	Ω
R_O Mismatch Between A and B	Δ R_O	V_{CM} = 1.0 V and 1.4 V	—	—	10	%
Change in Differential Voltage between Complementary States	$\lvert \Delta V_{OD} \rvert$	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
Change in Output Offset Voltage Between Complementary States	Δ V_{OS}	R_{LOAD} = 100 Ω ± 1%	—	—	25	mV
Output Current	I_{SA}, I_{SB}	Driver shorted to GND	—	—	24	mA
Output Current	I_{SAB}	Drivers shorted together	—	—	12	mA
Power-off Output Leakage	|Ixa|, |Ixb|	V_{DD} = 0 V V_{PAD}, V_{PADN} = 0 V—2.5 V	—	—	10	mA

* $V_{DD}33$ = 3.1 V—3.5 V, $V_{DD}15$ = 1.4 V—1.6 V, –40 °C, and slow-fast process.
† External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%.

Table 7. Driver ac Data*

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{OD} Fall Time, 80% to 20%	t_F	Z_L = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PAD} = 3.0 pF	100	210	ps
V_{OD} Rise Time, 20% to 80%	t_R	Z_L = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PAD} = 3.0 pF	100	210	ps
Differential Skew |t_{PHLA} – t_{PLHB}| or |t_{PHLB} – t_{PLHA}|	t_{SKEW1}	Any differential pair on package at 50% point of the transition	—	50	ps
Channel-to-channel Skew |tpDIFFm – tpDIFFn|,	t_{SKEW2}	Any two signals on package at 0 V differential	—	—	ps
Propagation Delay Time	t_{PLH} t_{PHL}	Z_L = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF	0.54 0.55	1.10 1.09	ns ns

* $V_{DD}33$ = 3.1 V—3.5 V, $V_{DD}15$ = 1.4 V—1.6 V, –40 °C, and slow-fast process.

Table 8. Driver Power Consumption*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver dc Power	PDdc	Z_L = 100 Ω ± 1%	—	26.0	mW
Driver ac Power	PDac	Z_L = 100 Ω ± 1% C_{PAD} = 3.0 pF, C_{PADN} = 3.0 pF	—	64	µW/MHz

* $V_{DD}33$ = 3.1 V—3.5 V, $V_{DD}15$ = 1.4 V—1.6 V, –40 °C, and slow-fast process.

Embedded Core LVDS I/O (continued)

LVDS Receiver Buffer Requirements

Table 9. Receiver ac Data*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Pulse-width Distortion	t_{pwd}	V_{IDTH} = 100 mV, 311 MHz	—	160	ps
Propagation Delay Time	t_{PLH} t_{PHL}	C_L = 0.5 pF	0.60 0.60	1.42 1.47	ns ns
With Common-mode Variation (0 V to 2.4 V)	$\lvert\Delta t_{PD}\rvert$	C_L = 0.5 pF	—	50	ps
Output Rise Time, 20% to 80%	t_R	C_L = 0.5 pF	150	350	ps
Output Fall Time, 80% to 20%	t_F	C_L = 0.5 pF	150	350	ps

* V_{DD} = 3.1 V—3.5 V, 0 °C—125 °C, slow-fast process.

Table 10. Receiver Power Consumption*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Receiver dc Power	P_{Rdc}	dc	—	20.4	mW
Receiver ac Power	P_{Rac}	ac C_L = 1.5 pF	—	4.5	µW/ MHz

* V_{DD} = 3.1 V—3.5 V, 0 °C—125 °C, slow-fast process.

Table 11. Receiver dc Data*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range, VIA or VIB	V_I	$\lvert V_{GPD}\rvert$ < 925 mV dc – 1 MHz	0.0	1.2	2.4	V
Input Differential Threshold	V_{IDTH}	$\lvert V_{GPD}\rvert$ < 925 mV 400 MHz	–100	—	100	mV
Input Differential Hysteresis	V_{HYST}	(+V_{IDTHH}) – (–V_{IDTHL})	—	—	— †	mV
Receiver Differential Input Impedance	R_{IN}	With build-in termination, center-tapped	80	100	120	Ω

* V_{DD} = 3.1 V—3.5 V, 0 °C—125 °C, slow-fast process.
† External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%.

Table 12. LVDS Operating Parameters

Parameter	Test Conditions	Min	Normal	Max	Unit
Transmit Termination Resistor	—	80	100	120	Ω
Receiver Termination Resistor	—	80	100	120	Ω
Temperature Range	—	–40	—	125	°C
Power Supply $V_{DD}33$	—	3.1	—	3.5	V
Power Supply $V_{DD}15$	—	1.4	—	1.6	V
Power Supply V_{SS}	—	—	0	—	V

Note: Under worst-case operating condition, the LVDS driver will withstand a disabled or unpowered receiver for an unlimited period of time without being damaged. Similarly, when outputs are short-circuited to each other or to ground, the LVDS will not suffer permanent damage. The LVDS driver supports hot-insertion. Under a well-controlled environment, the LVDS I/O can drive backplane as well as cable.

Timing Characteristics

Receive/Transmit Input Data/Sync Interface

Receive (Line)/Transmit (System) STS-48/STS-192 (2.5G/10G) Data Inputs

Figure 19 illustrates the timing for the receive (line) and transmit (system) STS-48/STS-192 data stream. Both the clock and data pins are low-voltage differential signal (LVDS) input buffers. The expected clock rate is 622.08 MHz/ 666.51428 MHz and the receive/transmit data is clocked on the rising edge of the clock. In 2.5G (divide-by-8) mode, each of the four channels uses one set of RX_CLK_IN_n and 4 RX_DAT_IN_n data pins. In 10G (divide-by-4) mode, only RX_CLK_IN_0 and TX_CLK_IN is used, along with theRX_DAT_IN_[15:0] pins.

Both the clock and frame sync are low-voltage differential signal (LVDS) input buffers. The expected clock is 622.08 MHz—666.51 MHz. It is recommended that the Rx clock be inverted by crossing the LVDS pin pair, that is, connect the N to the P and the P to the N. This is because the embedded LI requires the Rx data to be centered on the Rx clock. The timing values for the diagram are given in Table 13.

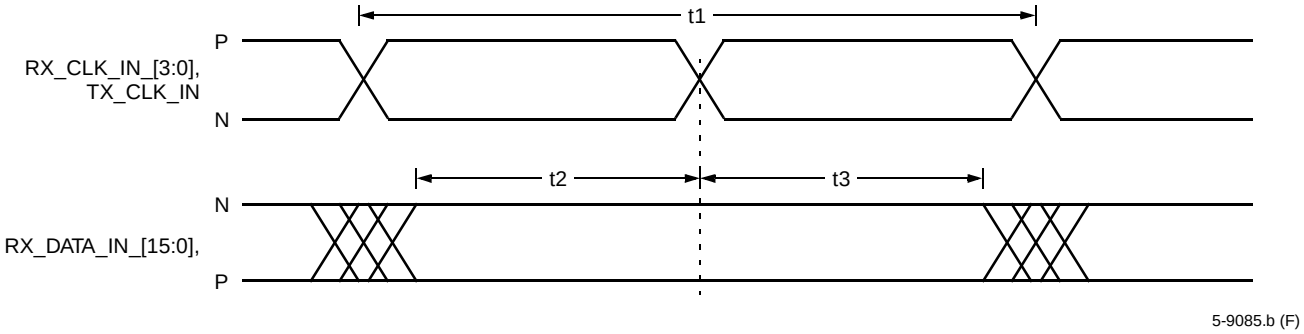


Figure 19. Receive/Transmit Data Timing

Table 13. Receive (Line)/Transmit (System) Data Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Clock Period	—	1608/1500	—	ps
t2	Data Setup Time Required	300	—	—	ps
t3	Data Hold Time Required	300	—	—	ps

Timing Characteristics (continued)

Transmit (Line)/Receive (System) STS-48/STS-192 (2.5G/10G) Data Outputs

Figure 20 illustrates the timing for the transmit (line)/receive (system) STS-48/STS-192 data stream. Both the clock and data pins are driven with low-voltage differential signal buffers. The expected clock rate is 622.08 MHz/ 666.51428 MHz and the receive/transmit data is clocked out on the rising edge of the clock. In 2.5G mode, each of the four channesl uses one set of TX_CLK_OUT_n with four TX_DAT_OUT_n data pins. In 10G mode, only TX_CLK_OUT[0] is used with the 16 TX_DAT_OUT pins. The timing values for the diagram are given in Table 14.

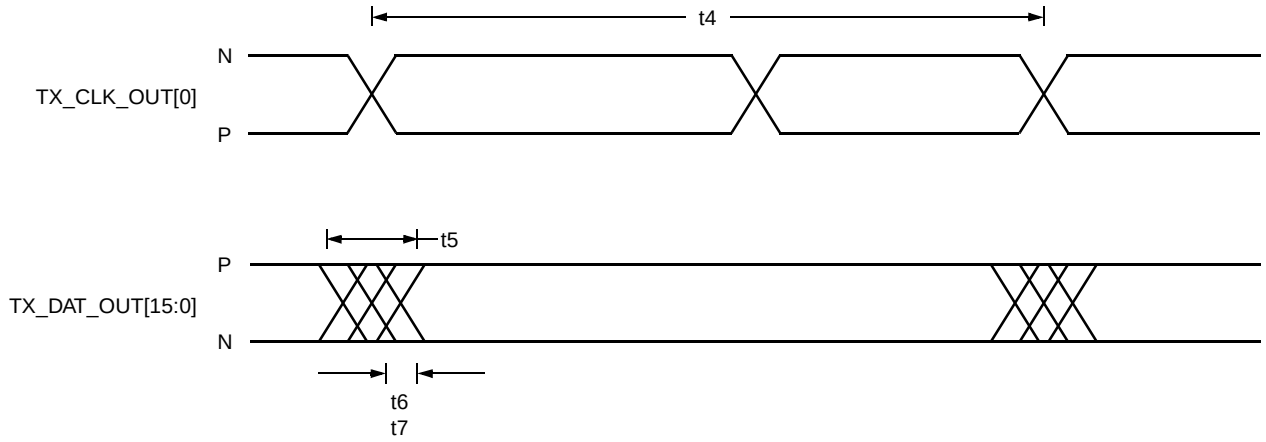


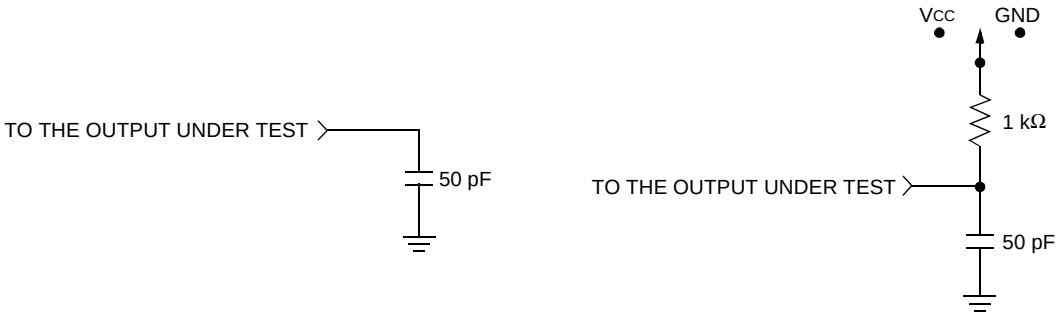
Figure 20. Transmit (Line)/Receive (System) Data Timing

Table 14. Transmit (Line)/Receive (System) Data Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t4	Clock Period	—	1608/1500	—	ps
—	Duty Cycle[1]	45	50	55	%
t5	Data Delay from Clock Edge	–220	—	220	ps
t6	Data Rise Time: 20%—80%	100	—	200	ps
t7	Data Fall Time: 80%—20%	100	—	200	ps
—	Clock In to Clock Out	1500	—	4500	ps

1. This requirement is for all sources of the output clocks (e.g., RCLKSI, etc.).

Input/Output Buffer Measurement Conditions (On-LVDS Buffer)

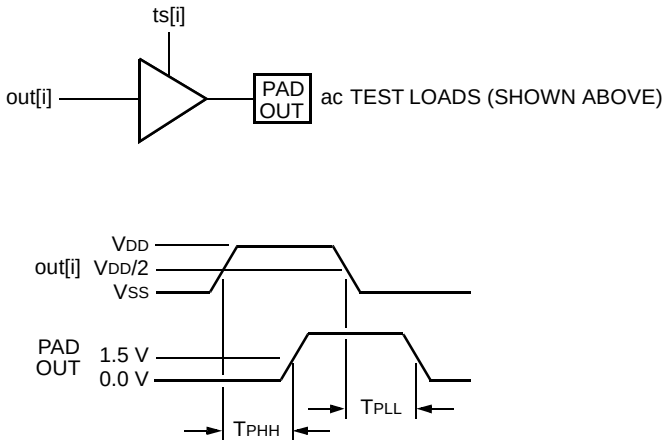


A. Load Used to Measure Propagation Delay **B. Load Used to Measure Rising/Falling Edges**

Note: Switch to V_{DD} for T_{PLZ}/T_{PZL}; switch to GND for T_{PHZ}/T_{PZH}.

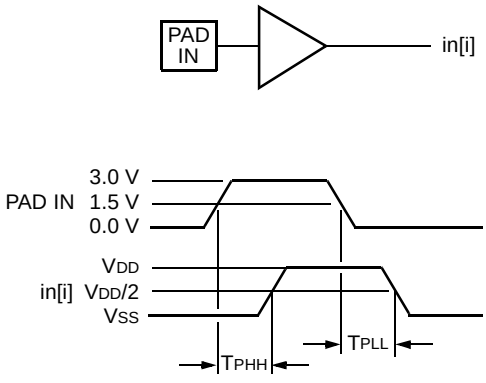
5-3234(F)

Figure 21. ac Test Loads



5-3233.a(F)

Figure 22. Output Buffer Delays



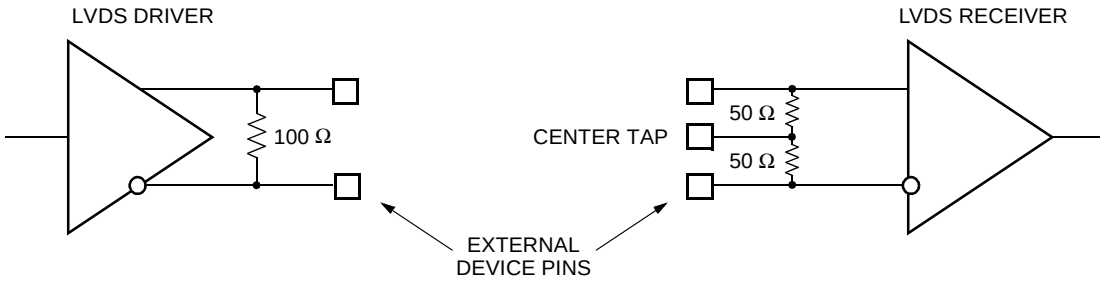
5-3235(F)

Figure 23. Input Buffer Delays

LVDS Buffer Characteristics

Termination Resistor

The LVDS drivers and receivers operate on a 100 Ω differential impedance, as shown below. External resistors are not required. The differential driver and receiver buffers include termination resistors inside the device package as shown in Figure 24 below.

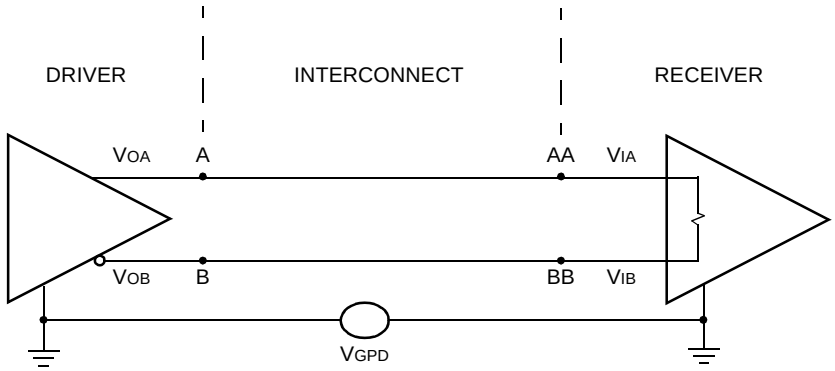


5-8703(F)

Figure 24. LVDS Driver and Receiver and Associated Internal Components

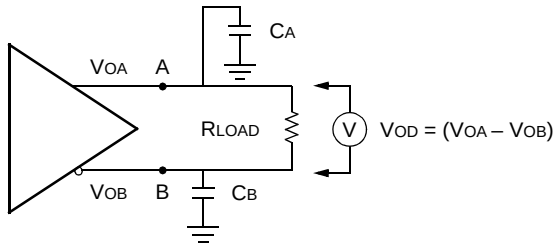
LVDS Driver Buffer Capabilities

Under worst-case operating condition, the LVDS driver must withstand a disabled or unpowered receiver for an unlimited period of time without being damaged. Similarly, when its outputs are short-circuited to each other or to ground, the LVDS driver will not suffer permanent damage. Figure 25 illustrates the terms associated with LVDS driver and receiver pairs.



5-8704(F)

Figure 25. LVDS Driver and Receiver



5-8705(F)

Figure 26. LVDS Driver

Pin Information

This section describes the pins and signals that perform FPGA-related functions. During configuration, the user-programmable I/Os are 3-stated and pulled-up with an internal resistor. If any FPGA function pin is not used (or not bonded to package pin), it is also 3-stated and pulled-up after configuration.

Table 15. FPGA Common-Function Pin Description

Symbol	I/O	Description
Dedicated Pins		
$V_{DD}33$	—	3 V positive power supply.
$V_{DD}15$	—	1.5 V positive power supply for internal logic.
V_{DDIO}	—	Positive power supply used by I/O banks.
GND	—	Ground supply.
PTEMP	I	Temperature-sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	I O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in. In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.*
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
$\overline{\text{PRGM}}$	I	$\overline{\text{PRGM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
$\overline{\text{RD\_CFG}}$	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/$\overline{\text{MPI\_IRQ}}$	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output.

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 15. FPGA Common-Function Pin Description (continued)

Symbol	I/O	Description
Special-Purpose Pins (Can also be used as a general I/O.)		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of INIT. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.*
PLL_CK[0:1,6:7]	I/O	Dedicated PCM clock pins. These pins are a user-programmable I/O pins if not used by PLLs.
P[TBLR]CLK[1:0][TC]	I/O	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing. They may be used as general I/O pins if not needed for clocking purposes.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O.*
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. After configuration, if the MPI is not used, this pin is a user-programmable I/O pin.*
	I/O	During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
HDC	O	High during configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{LDC}}$	O	$\overline{\text{Low during configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low, open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O pins.*
$\overline{\text{RD}}$/MPI_$\overline{\text{STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D7 into a status output. As a status indication, a high indicates ready, and a low indicates busy. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe.
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin.*

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 15. FPGA Common-Function Pin Description (continued)

Symbol	I/O	Description
A[17:0]	I	During MPI mode, the A[17:0] are used as the address bus driven by the *PowerPC* bus master utilizing the least significant bits of the *PowerPC* 32-bit address.
	O	During master parallel configuration mode, A[17:0] address the configuration EPROM. In MPI mode, many of the A[n] pins have alternate uses as described below. See the special function blocks section for more MPI information. During configuration, if not in master parallel or an MPI configuration mode, these pins are 3-stated with a pull-up enabled.
$\overline{\text{MPI\_BURST}}$		A[21] is used as the $\overline{\text{MPI\_BURST}}$. It is driven low to indicate a burst transfer is in progress. Driven high indicates that the current transfer is not a burst.
$\overline{\text{MPI\_BDIP}}$		A[20] is used as the $\overline{\text{MPI\_BDIP}}$. It is driven by the *PowerPC* processor assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[1:0]		A[19:18] are used as the MPI_TSZ[1:0] signals and are driven by the bus master to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]		During master parallel mode A[21:0], address the configuration EPROMs up to 4 Mbytes. If not used for MPI, these pins are user-programmable I/O pins.*
$\overline{\text{MPI\_ACK}}$	O	In *PowerPC* mode MPI operation, this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
$\overline{\text{MPI\_CLK}}$	I	This is the *PowerPC* synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the embedded system bus. If MPI is used, this can be the *AMBA* bus clock.
$\overline{\text{MPI\_TEA}}$	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
$\overline{\text{MPI\_RTRY}}$	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
D[31:0]	I/O	Selectable data bus width from 8-, 16-, 32-bit. Driven by the bus master in a write transaction. Driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input. D[7:3] output internal status for asynchronous peripheral mode when RD is low. After configuration, the pins are user-programmable I/O pins.*
DP[3:0]	I/O	Selectable parity bus width from 1, 2, 4-bit, DP[0] for D[7:0], DP[1] for D[15:8], DP[2] for D[23:16], and DP[3] for D[32:24]. After configuration, this pin is a user-programmable I/O pin.*
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.*

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

This table describes the I/O signal ports on the embedded core portion of the device.

Table 16. FPSC Function Pin Description

Symbol	I/O	Description
Control and Global Pins		
PLL_BYPASS	I	3.3 V Active-high. Enables the bypass mode for both receive and both transmit PLLs.
PWRDN	I	3.3 V Active-high. Power down all LVDS links and both receive and both transmit PLLs.
RESET_RX	I	3.3 V Active-high. Resets the receive PLLs and the demultiplexer block.
RESET_TX	I	3.3 V Active-high. Resets the transmit PLLs and the multiplexer block.
Receive I/O Pins		
RX_DAT_IN_N<15:0>	I	LVDS data input for receive side.
RX_DAT_IN_P<15:0>	I	LVDS data input for receive side.
RX_CLK_IN_N<3:0>	I	LVDS clock inputs for receive side.
RX_CLK_IN_P<3:0>	I	LVDS clock inputs for receive side.
Transmit I/O Pins		
TX_DAT_OUT_N<15:0>	O	LVDS data outputs on transmit side.
TX_DAT_OUT_N<15:0>	O	LVDS data outputs on transmit side.
TX_CLK_OUT_N<3:0>	O	LVDS clock outputs on transmit side.
TX_CLK_OUT_N<3:0>	O	LVDS clock outputs on transmit side.
TX_CLK_IN_N	I	LVDS transmit reference clock input.
TX_CLK_IN_P	I	LVDS transmit reference clock input.
LVDS Input Reference Pins		
LV_REF10	—	LVDS reference voltage: 1.0 V ± 3%
LV_REF14	—	LVDS reference voltage: 1.4 V ± 3%
LV_RESHI	—	LVDS resistor high pin (use 100 Ω to LV_RESLO pin).
LV_RESLO	—	LVDS resistor low pin (use 100 Ω to LV_RESHI pin).
LVCTAP_[6:1]	—	LVDS input centertap (use 0.01 µF to GND).

Pin Information (continued)

In Table 17, an input refers to a signal flowing into the FGPA logic (out of the embedded core) and an output refers to a signal flowing out of the FPGA logic (into the embedded core).

Table 17. Embedded Core/FPGA Interface Signal Description

Pin Name	I/O	Description
Receive Signals		
RX_DAT_OUT<127:0>	O	Data from demultiplexer on receive side.
RX_CLK8_OUT<3:0>	O	Divided down clocks on receive side.
RX_ENB8_OUT<3:0>	O	Data enables on receive side.
RX1_VCOP	O	RX1_PLL output clock on receive side (M/N clock).
RX2_VCOP	O	RX1_PLL output clock on receive side (x1 clock).
RX_LOCK	O	Lock signal for RX1_PLL and RX2_PLL.
Transmit Signals		
TX_DAT_IN<127:0>	I	Data to multiplexer on transmit side.
TX_CLK8_IN<3:0>	I	Clocks to multiplexer on transmit side.
TX_ENB_IN	I	Data enables on transmit side.
TX1_VCOP	O	TX1_PLL output clock on transmit side (M/N clock).
TX2_VCOP	O	TX1_PLL output clock on transmit side (x1 clock).
TX_LOCK	O	Lock signal for TX1_PLL and TX2_PLL.
Vss_A<7:4>	—	Analog ground for the embedded line interface PLLs.
V_{DD}33_A<7:4>	—	Analog power supply for the embedded line interface PLLs.

Pin Information (continued)

Package Pinouts

Table 15 provides the number of user programmable I/Os available for each available package.

Table 19 provides the package pin and pin function for the ORLI10G FPSC and packages. The bond pad name is identified in the PIO nomeclature used in the *ORCA* Foundry design editor. The bank column provides information as to which output voltage level bank the given pin is in. The group column provides information as to the group of pins the given pin is in. This is used to show which VREF pin is used to provide the reference voltage for single-ended limited-swing I/Os. If none of these buffer types (such as SSTL, GTL, HSTL) are used in a given group, then the VREF pin is available as an I/O pin.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects). When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the device column for the FPGA. The tables provide no information on unused pads.

Table 18*. ORCA* Programmable I/Os Summary

Device	416 PBGAM1	680 PBGAM1
user programmable I/O	192	316
Available programmable differential pairs	184	272
FPGA configuration pins	7	7
FPGA dedicated function pins	2	2
Core function pins	86	86
VDD15	28	84
VDD33_A	4	4
VDDIO	21	44
VSS	48	95
VSS_A	4	4
LVCTAP For dedicated differential channels	6	6
Core LV_REF pins	4	4
Total Package pins	416	680

It is very important to note the pinout limitations for 10 Gbits/s Ethernet applications. Specifically, the very stringent timing requirements of the XGMII specification coupled with the I/O availability and locations in the 416-pin PBGA requires that the XGMII output pins be located on three sides of the device. This may cause issues with routing the XGMII bus at a board level as the XGMII specification for routing this bus on a board is only 2 in.

In addition, the built-in microprocessor interface (MPI) cannot be fully utilized in the 416-pin PBGA and the 680-pin PBGA packages because the implementation of the XGMII interface limits the number of available address and data pins.

As shown in the Pair columns in Table 19, differential pairs and physical locations are numbered within each bank (e.g., L19C_A0 is the nineteenth pair in an associated bank). A C indicates complementary differential whereas a T indicates true differential. An _A0 indicates the physical location of adjacent balls in either the horizontal or vertical direction. Other physical indicators are as follows:

- _A1 indicates one ball between pairs.
- _A2 indicates two balls between pairs.
- _D0 indicates balls are diagonally adjacent.
- _D1 indicates balls are diagonally adjacent separated by one physical ball.

VREF pins, shown in the Pin Description column in Table 19, are associated to the bank and group (e.g., VREF_TL_01 is the VREF for group one of the top left (TL) bank).

Pin Information (continued)

Table 19. PBGA Pinout Table

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
D4	E5	—	—	$V_{DD}33$	—	—
D3	E4	—	—	PRD_DATA/TDO	—	—
A1	PLANE	—	—	$V_{DD}15$	—	—
C1	C1	—	—	$\overline{\text{PRESET}}$	—	—
E4	D1	—	—	$\overline{\text{PRD\_CFG}}$	—	—
F4	E2	—	—	$\overline{\text{PPRGRM}}$	—	—
D2	F4	V_{DDIO}0_TL	7	PL2D/PLL_CK0C	L14C_D0	L21C_A0
E3	F3	V_{DDIO}0_TL	7	PL2C/PLL_CK0T	L14T_D0	L21T_A0
NC	G5	V_{DDIO}0_TL	7	PL3D	—	L22C_A0
D1	F5	V_{DDIO}0_TL	7	PL3C/VREF_TL_07	—	L22T_A0
E2	G4	V_{DDIO}0_TL	7	PL4D/D5	L15C_D0	L23C_D1
F3	F2	V_{DDIO}0_TL	7	PL4C/D6	L15T_D0	L23T_D1
NC	H5	V_{DDIO}0_TL	8	PL4B	—	L24C_D1
NC	G3	V_{DDIO}0_TL	8	PL4A/VREF_TL_08	—	L24T_D1
E1	F1	V_{DDIO}0_TL	8	PL5D/HDC	L16C_D0	L25C_A0
F2	G2	V_{DDIO}0_TL	8	PL5C/$\overline{\text{LDC}}$	L16T_D0	L25T_A0
NC	H4	V_{DDIO}0_TL	8	PL5B	—	L26C_A0
NC	J5	V_{DDIO}0_TL	8	PL5A	—	L26T_A0
G4	H3	V_{DDIO}0_TL	9	PL6D	L17C_A0	L27C_D1
H4	G1	V_{DDIO}0_TL	9	PL6C/D7	L17T_A0	L27T_D1
F1	J4	V_{DDIO}0_TL	9	PL7D/VREF_TL_09	L18C_D0	L28C_D1
G2	H2	V_{DDIO}0_TL	9	PL7C/A17	L18T_D0	L28T_D1
H2	K5	V_{DDIO}0_TL	9	PL8D/$\overline{\text{CS0}}$	L19C_A0	L29C_D1
H3	J3	V_{DDIO}0_TL	9	PL8C/CS1	L19T_A0	L29T_D1
G1	H1	V_{DDIO}0_TL	1	PL9D	L20C_A0	L30C_A0
H1	J2	V_{DDIO}0_TL	1	PL9C	L20T_A0	L30T_A0
NC	K4	V_{DDIO}0_TL	1	PL9A	—	—
J4	L5	V_{DDIO}0_TL	1	PL10D/$\overline{\text{INIT}}$	L21C_A0	L31C_D1
K4	K3	V_{DDIO}0_TL	1	PL10C/DOUT	L21T_A0	L31T_D1
A26	PLANE	—		$V_{DD}15$	—	—
J3	J1	V_{DDIO}0_TL	1	PL11D/VREF_TL_10	L22C_A0	L32C_A0
J2	K2	V_{DDIO}0_TL	1	PL11C/A16	L22T_A0	L32T_A0
NC	K1	V_{DDIO}0_TL	1	PL11A	—	—
J1	M5	V_{DDIO}7_CL	1	PL12D/A15	L1C_D0	L1C_A0
K2	L4	V_{DDIO}7_CL	1	PL12C/A14	L1T_D0	L1T_A0
NC	M4	V_{DDIO}7_CL	1	PL12B	—	L2C_A0
NC	N5	V_{DDIO}7_CL	1	PL12A	—	L2T_A0
K3	L3	V_{DDIO}7_CL	1	PL13D/VREF_CL_01	L2C_A0	L3C_A0
L3	L2	V_{DDIO}7_CL	1	PL13C/D4	L2T_A0	L3T_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	N4	V_{DDIO}7_CL	2	PL13B	—	L4C_A0
NC	P5	V_{DDIO}7_CL	2	PL13A	—	L4T_A0
L4	M2	V_{DDIO}7_CL	2	PL14D/RDY/$\overline{BUSY}$/RCLK	L3C_A0	L5C_A0
M4	M1	V_{DDIO}7_CL	2	PL14C/VREF_CL_02	L3T_A0	L5T_A0
L1	N3	V_{DDIO}7_CL	2	PL15D/A13	L4C_A0	L6C_A0
M1	N2	V_{DDIO}7_CL	2	PL15C/A12	L4T_A0	L6T_A0
M3	P4	V_{DDIO}7_CL	3	PL16D	L5C_A0	L7C_A0
M2	P3	V_{DDIO}7_CL	3	PL16C	L5T_A0	L7T_A0
NC	R5	V_{DDIO}7_CL	3	PL16A	—	—
N1	N1	V_{DDIO}7_CL	3	PL17D/A11	L6C_A0	L8C_A0
N2	P2	V_{DDIO}7_CL	3	PL17C/VREF_CL_03	L6T_A0	L8T_A0
NC	R4	V_{DDIO}7_CL	3	PL17A	—	—
NC	P1	V_{DDIO}7_CL	3	PL18D	—	L9C_A0
NC	R2	V_{DDIO}7_CL	3	PL18C	—	L9T_A0
U14	PLANE	—	—	V_{DD}15	—	—
NC	R1	V_{DDIO}7_CL	3	PL18A	—	L10T_A0
NC	T2	V_{DDIO}7_CL	3	PL18B	—	L10C_A0
N3	T5	V_{DDIO}7_CL	4	PL19D/$\overline{RD}$/$\overline{MPI_STRB}$	L7C_A0	L11C_A0
N4	T4	V_{DDIO}7_CL	4	PL19C/VREF_CL_04	L7T_A0	L11T_A0
NC	T3	V_{DDIO}7_CL	4	PL19A	—	L12T_D1
NC	U5	V_{DDIO}7_CL	4	PL19B	—	L12C_D1
P4	T1	V_{DDIO}7_CL	4	PL20D/PLCK0C	L8C_A0	L13C_D1
P3	U3	V_{DDIO}7_CL	4	PL20C/PLCK0T	L8T_A0	L13T_D1
NC	U4	V_{DDIO}7_CL	4	PL20B	—	L14C_A1
NC	U2	V_{DDIO}7_CL	4	PL20A	—	L14T_A1
P1	V1	V_{DDIO}7_CL	5	PL21D/A10	L9C_A0	L15C_A0
R1	V2	V_{DDIO}7_CL	5	PL21C/A9	L9T_A0	L15T_A0
NC	V3	V_{DDIO}7_CL	5	PL21B	—	L16C_A0
NC	V4	V_{DDIO}7_CL	5	PL21A	—	L16T_A0
R2	V5	V_{DDIO}7_CL	5	PL22D/A8	L10C_A0	L17C_A0
R3	W4	V_{DDIO}7_CL	5	PL22C/VREF_CL_05	L10T_A0	L17T_A0
AF26	PLANE	—	—	V_{DD}15	—	—
NC	W3	V_{DDIO}7_CL	5	PL23D	—	L18C_A0
NC	W2	V_{DDIO}7_CL	5	PL23C	—	L18T_A0
NC	Y1	V_{DDIO}7_CL	5	PL23A	—	—
T1	W5	V_{DDIO}7_CL	6	PL24D/PLCK1C	L11C_A0	L19C_A0
T2	Y4	V_{DDIO}7_CL	6	PL24C/PLCK1T	L11T_A0	L19T_A0
NC	Y2	V_{DDIO}7_CL	6	PL24A	—	—
T4	Y5	V_{DDIO}7_CL	6	PL25D/VREF_CL_06	L12C_A0	L20C_D1

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
R4	AA3	V_{DDIO}7_CL	6	PL25C/A7	L12T_A0	L20T_D1
NC	AA2	V_{DDIO}7_CL	6	PL25A	—	—
U1	AA1	V_{DDIO}7_CL	6	PL26D/A6	L13C_A0	L21C_A0
U2	AB1	V_{DDIO}7_CL	6	PL26C/A5	L13T_A0	L21T_A0
V1	AA4	V_{DDIO}7_CL	7	PL26B	—	—
V2	AB2	V_{DDIO}7_CL	7	PL27D/$\overline{WR}$/MPI_RW	L14C_D0	L22C_A0
U3	AB3	V_{DDIO}7_CL	7	PL27C/VREF_CL_07	L14T_D0	L22T_A0
NC	AA5	V_{DDIO}7_CL	7	PL27B	—	L23C_A0
NC	AB4	V_{DDIO}7_CL	7	PL27A	—	L23T_A0
W1	AC2	V_{DDIO}7_CL	8	PL28D/A4	L15C_A0	L23C_A0
Y1	AC1	V_{DDIO}7_CL	8	PL28C/VREF_CL_08	L15T_A0	L23T_A0
V4	AB5	V_{DDIO}7_CL	8	PL29D/A3	L16C_A0	L23C_A0
U4	AC4	V_{DDIO}7_CL	8	PL29C/A2	L16T_A0	L23T_A0
NC	AD2	V_{DDIO}7_CL	8	PL29A	—	—
V3	AC5	V_{DDIO}7_CL	8	PL30D/A1	L17C_D0	L24C_D1
W2	AD3	V_{DDIO}7_CL	8	PL30C/A0	L17T_D0	L24T_D1
Y2	AE1	V_{DDIO}7_CL	8	PL31D/DP0	L18C_D0	L25C_A0
W3	AE2	V_{DDIO}7_CL	8	PL31C/DP1	L18T_D0	L25T_A0
NC	AF1	V_{DDIO}7_CL	8	PL31A	—	—
AA1	AD5	V_{DDIO}6_BL	1	PL32D/D8	L1C_A0	L1C_A0
AA2	AD4	V_{DDIO}6_BL	1	PL32C/VREF_BL_01	L1T_A0	L1T_A0
NC	AE3	V_{DDIO}6_BL	1	PL32A	—	—
Y3	AE5	V_{DDIO}6_BL	1	PL33D/D9	L2C_D0	L2C_A0
W4	AE4	V_{DDIO}6_BL	1	PL33C/D10	L2T_D0	L2T_A0
Y4	AF2	V_{DDIO}6_BL	2	PL34D	L3C_D0	L3C_A0
AA3	AG1	V_{DDIO}6_BL	2	PL34C/VREF_BL_02	L3T_D0	L3T_A0
NC	AF3	V_{DDIO}6_BL	2	PL34B	—	L4C_A1
NC	AF5	V_{DDIO}6_BL	2	PL34A	—	L4T_A1
AB2	AG2	V_{DDIO}6_BL	3	PL35B/D11	L4C_D0	L5C_D1
AC1	AF4	V_{DDIO}6_BL	3	PL35A/D12	L4T_D0	L5T_D1
NC	AH1	V_{DDIO}6_BL	3	PL36D	—	L6C_D1
NC	AG3	V_{DDIO}6_BL	3	PL36C	—	L6T_D1
AC2	AH2	V_{DDIO}6_BL	3	PL36B/VREF_BL_03	L5C_D0	L7C_A0
AB3	AJ1	V_{DDIO}6_BL	3	PL36A/D13	L5T_D0	L7T_A0
NC	AG4	V_{DDIO}6_BL	4	PL37D	—	—
NC	AH3	V_{DDIO}6_BL	4	PL37B	—	L8C_D1
AD1	AG5	V_{DDIO}6_BL	4	PL37A/VREF_BL_04	—	L8T_D1
NC	AJ2	V_{DDIO}6_BL	4	PL38C	—	—
NC	AK1	V_{DDIO}6_BL	4	PL38B	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	AH4	V_{DDIO}6_BL	4	PL38A	—	—
AA4	AJ3	V_{DDIO}6_BL	4	PL39D/PLL_CK7C	L6C_A0	L9C_A0
AB4	AK2	V_{DDIO}6_BL	4	PL39C/PLL_CK7T	L6T_A0	L9T_A0
NC	AH5	V_{DDIO}6_BL	4	PL39B	—	L10C_A0
NC	AJ4	V_{DDIO}6_BL	4	PL39A	—	L10T_A0
AC3	AK3	—	—	PTEMP	—	—
R14	PLANE	—	—	V_{DD}15	—	—
AE2	AN1	—	—	LVDS_R	—	—
AD3	AJ5	—	—	V_{DD}33	—	—
AC4	AL5	—	—	V_{DD}33	—	—
T13	PLANE	—	—	V_{DD}15	—	—
AE3	AM5	V_{DDIO}6_BL	5	PB2A/DP2	—	L11T_A0
NC	AN4	V_{DDIO}6_BL	5	PB2B	—	L11C_A0
AC5	AK6	V_{DDIO}6_BL	5	PB2C/PLL_CK6T	L7T_D0	L12T_A0
AD4	AL6	V_{DDIO}6_BL	5	PB2D/PLL_CK6C	L7C_D0	L12C_A0
NC	AK7	V_{DDIO}6_BL	5	PB3A	—	—
NC	AN5	V_{DDIO}6_BL	5	PB3C	—	L13T_A0
NC	AM6	V_{DDIO}6_BL	5	PB3D	—	L13C_A0
AE4	AN6	V_{DDIO}6_BL	5	PB4A/VREF_BL_05	L8T_D0	L14T_A0
AF3	AP5	V_{DDIO}6_BL	5	PB4B/DP3	L8C_D0	L14C_A0
AC6	AL7	V_{DDIO}6_BL	6	PB4C	L9T_D0	L15T_A0
AD5	AM7	V_{DDIO}6_BL	6	PB4D	L9C_D0	L15C_A0
AF4	AN7	V_{DDIO}6_BL	6	PB5C/VREF_BL_06	L10T_D0	L16T_A0
AE5	AP6	V_{DDIO}6_BL	6	PB5D/D14	L10C_D0	L16C_A0
NC	AK8	V_{DDIO}6_BL	6	PB6A	—	L17T_A0
AD6	AL8	V_{DDIO}6_BL	6	PB6B	—	L17C_A0
AC7	AM8	V_{DDIO}6_BL	7	PB6C/D15	L11T_A0	L18T_D1
AC8	AK9	V_{DDIO}6_BL	7	PB6D/D16	L11C_A0	L18C_D1
NC	AP7	V_{DDIO}6_BL	7	PB7A	—	—
AD7	AL9	V_{DDIO}6_BL	7	PB7C/D17	L12T_D0	L19T_A0
AE6	AK10	V_{DDIO}6_BL	7	PB7D/D18	L12C_D0	L19C_A0
NC	AN8	V_{DDIO}6_BL	7	PB8A	—	—
AE7	AM9	V_{DDIO}6_BL	7	PB8C/VREF_BL_07	L13T_D0	L20T_A0
AD8	AL10	V_{DDIO}6_BL	7	PB8D/D19	L13C_D0	L20C_A0
NC	AP8	V_{DDIO}6_BL	8	PB9A	—	—
AF6	AL11	V_{DDIO}6_BL	8	PB9C/D20	L14T_A0	L21T_A0
AF7	AK11	V_{DDIO}6_BL	8	PB9D/D21	L14C_A0	L21C_A0
NC	AM10	V_{DDIO}6_BL	8	PB10A	—	—
AE8	AN9	V_{DDIO}6_BL	8	PB10C/VREF_BL_08	L15T_D0	L22T_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
T14	PLANE	—	—	$V_{DD}15$	—	—
AD9	AP9	$V_{DDIO}6\_BL$	8	PB10D/D22	L15C_D0	L22C_A0
NC	AM11	$V_{DDIO}6\_BL$	9	PB11A	—	L23T_D1
NC	AK12	$V_{DDIO}6\_BL$	9	PB11B	—	L23C_D1
AC9	AN10	$V_{DDIO}6\_BL$	9	PB11C/D23	L16T_A0	L24T_A0
AC10	AP10	$V_{DDIO}6\_BL$	9	PB11D/D24	L16C_A0	L24C_A0
NC	AL12	$V_{DDIO}6\_BL$	9	PB12A	—	L25T_A0
NC	AK13	$V_{DDIO}6\_BL$	9	PB12B	—	L25C_A0
AF8	AN11	$V_{DDIO}6\_BL$	9	PB12C/VREF_BL_09	L17T_D0	L26T_A0
AE9	AN12	$V_{DDIO}6\_BL$	9	PB12D/D25	L17C_D0	L26C_A0
NC	AK14	$V_{DDIO}6\_BL$	9	PB13A	—	L27T_A0
NC	AL13	$V_{DDIO}6\_BL$	9	PB13B	—	L27C_A0
AD10	AP12	$V_{DDIO}6\_BL$	1	PB13C/D26	L18T_A0	L28T_A0
AE10	AN13	$V_{DDIO}6\_BL$	1	PB13D/D27	L18C_A0	L28C_A0
NC	AL14	$V_{DDIO}6\_BL$	1	PB14A	—	L29T_A0
NC	AK15	$V_{DDIO}6\_BL$	1	PB14B	—	L29C_A0
AE11	AP13	$V_{DDIO}6\_BL$	1	PB14C/VREF_BL_10	L19T_A0	L30T_A0
AD11	AP14	$V_{DDIO}6\_BL$	1	PB14D/D28	L19C_A0	L30C_A0
NC	AN14	$V_{DDIO}6\_BL$	11	PB15A	—	—
AC12	AM14	$V_{DDIO}6\_BL$	11	PB15C/D29	L20T_A0	L31T_A0
AC11	AL15	$V_{DDIO}6\_BL$	11	PB15D/D30	L20C_A0	L31C_A0
NC	AN15	$V_{DDIO}6\_BL$	11	PB16A	—	—
AF10	AM16	$V_{DDIO}6\_BL$	11	PB16C/VREF_BL_11	L21T_A0	L32T_A0
AF11	AL16	$V_{DDIO}6\_BL$	11	PB16D/D31	L21C_A0	L32C_A0
NC	AP15	$V_{DDIO}5\_BC$	1	PB17A	—	—
AD12	AN16	$V_{DDIO}5\_BC$	1	PB17C	L1T_A0	L1T_A0
AE12	AP16	$V_{DDIO}5\_BC$	1	PB17D	L1C_A0	L1C_A0
NC	AK16	$V_{DDIO}5\_BC$	1	PB18A	—	—
AF12	AL17	$V_{DDIO}5\_BC$	1	PB18C/VREF_BC_01	L2T_A0	L2T_A0
P16	PLANE	—	—	$V_{DD}15$	—	—
AF13	AK17	$V_{DDIO}5\_BC$	1	PB18D	L2C_A0	L2C_A0
NC	AM17	$V_{DDIO}5\_BC$	2	PB19A	—	L3T_A0
NC	AN17	$V_{DDIO}5\_BC$	2	PB19B	—	L3C_A0
AD13	AP18	$V_{DDIO}5\_BC$	2	PB19C/PBCK0T	L3T_A0	L4T_A1
AE13	AM18	$V_{DDIO}5\_BC$	2	PB19D/PBCK0C	L3C_A0	L4C_A1
NC	AL18	$V_{DDIO}5\_BC$	2	PB20B	—	L5C_A1
NC	AN18	$V_{DDIO}5\_BC$	2	PB20A	—	L5T_A1
AC14	AN19	$V_{DDIO}5\_BC$	2	PB20C/VREF_BC_02	L4T_A0	L6T_D2
AC13	AK18	$V_{DDIO}5\_BC$	2	PB20D	L4C_A0	L6C_2

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	AM19	V_{DDIO}5_BC	2	PB21A	—	L7T_D1
NC	AP20	V_{DDIO}5_BC	2	PB21B	—	L7C_D1
R13	PLANE	—	—	V_{DD}15	—	—
AE14	AL19	V_{DDIO}5_BC	3	PB21C	L5T_A0	L8T_D1
AD14	AN20	V_{DDIO}5_BC	3	PB21D/VREF_BC_03	L5C_A0	L8C_D1
NC	AP21	V_{DDIO}5_BC	3	PB22A	—	—
AF15	AL20	V_{DDIO}5_BC	3	PB22C	L6T_A0	L9T_A0
AE15	AK19	V_{DDIO}5_BC	3	PB22D	L6C_A0	L9C_A0
NC	AN21	V_{DDIO}5_BC	3	PB23A	—	—
AD15	AK20	V_{DDIO}5_BC	3	PB23C/PBCK1T	L7T_D0	L10T_D1
AE16	AM21	V_{DDIO}5_BC	3	PB23D/PBCK1C	L7C_D0	L10C_D1
NC	AP22	V_{DDIO}5_BC	3	PB24A	—	—
AC15	AL21	V_{DDIO}5_BC	4	PB24C	L8T_A0	L11T_D1
AC16	AN22	V_{DDIO}5_BC	4	PB24D	L8C_A0	L11C_D1
NC	AP23	V_{DDIO}5_BC	4	PB25A	—	—
AD16	AN23	V_{DDIO}5_BC	4	PB25C	L9T_D0	L12T_A0
AE17	AN24	V_{DDIO}5_BC	4	PB25D/VREF_BC_04	L9C_D0	L12C_A0
NC	AK21	V_{DDIO}5_BC	4	PB26A	—	L13T_A0
NC	AL22	V_{DDIO}5_BC	4	PB26B	—	L13C_A0
AF18	AP25	V_{DDIO}5_BC	5	PB26C	L10T_A0	L14T_D1
AE18	AM24	V_{DDIO}5_BC	5	PB26D/VREF_BC_05	L10C_A0	L14C_D1
NC	AK22	V_{DDIO}5_BC	5	PB27A	—	L15T_A0
NC	AL23	V_{DDIO}5_BC	5	PB27B	—	L15C_A0
AF19	AN25	V_{DDIO}5_BC	5	PB27C	L11T_A0	L16T_D1
AF20	AL24	V_{DDIO}5_BC	5	PB27D	L11C_A0	L16T_D1
NC	AP26	V_{DDIO}5_BC	6	PB28A	—	—
AC18	AM25	V_{DDIO}5_BC	6	PB28C	L12T_A0	L17T_D1
AC17	AK23	V_{DDIO}5_BC	6	PB28D/VREF_BC_06	L12C_A0	L17C_D1
NC	AN26	V_{DDIO}5_BC	6	PB29A	—	—
NC	AL25	V_{DDIO}5_BC	6	PB29C	—	L18T_A0
NC	AK24	V_{DDIO}5_BC	6	PB29D	—	L18C_A0
NC	AP27	V_{DDIO}5_BC	7	PB30A	—	—
AD18	AM26	V_{DDIO}5_BC	7	PB30C	L13T_D0	L19T_A0
AE19	AN27	V_{DDIO}5_BC	7	PB30D	L13C_D0	L19C_A0
AE20	AP28	V_{DDIO}5_BC	7	PB31C/VREF_BC_07	L14T_D0	L20T_D1
AD19	AM27	V_{DDIO}5_BC	7	PB31D	L14C_D0	L20C_D1
AF21	AL26	V_{DDIO}5_BC	7	PB32C	L15T_A0	L21T_A0
AE21	AK25	V_{DDIO}5_BC	7	PB32D	L15C_A0	L21C_A0
AC19	AN28	V_{DDIO}5_BC	8	PB33C	—	L22T_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	AP29	V_{DDIO}5_BC	8	PB33D/VREF_BC_08	—	L22C_A0
AF23	AK26	—	—	V_{DD}33	—	—
AC20	AL27	—	—	RX_DAT_IN_0_P	L1_D2	L1_A0
AF22	AM28	—	—	RX_DAT_IN_0_N	L1_D2	L1_A0
AE22	AN29	—	—	RX_DAT_IN_1_P	L2_D0	L2_A0
AD21	AP30	—	—	RX_DAT_IN_1_N	L2_D0	L2_A0
AE23	AL28	—	—	RX_DAT_IN_2_P	L3_D0	L3_A0
AF24	AM29	—	—	RX_DAT_IN_2_N	L3_D0	L3_A0
AC21	AK27	—	—	RX_DAT_IN_3_P	L4_D0	L4_A0
NC	AN30	—	—	V_{DD}33	—	—
AD22	AK28	—	—	RX_DAT_IN_3_N	L4_D0	L4_A0
AD23	AL29	—	—	RX_CLK_IN_0_P	L5_D0	L5_A0
AE24	AM30	—	—	RX_CLK_IN_0_N	L5_D0	L5_A0
AC22	AN31	—	—	LVCTAP_1	—	—
AC23	AP32	—	—	V_{SS}A_4	—	—
NC	PLANE	—	—	V_{DD}15	—	—
AD24	AK30	—	—	V_{DD}33A_4	—	—
AE25	AK31	—	—	V_{DD}33A_5	—	—
AC24	AJ30	—	—	V_{DD}33	—	—
AD25	AK32	—	—	V_{SS}A_5	—	—
AD26	AJ31	—	—	LVCTAP_2	—	—
NC	AH30	—	—	V_{DD}33	—	—
NC	PLANE	—	—	V_{DD}15	—	—
AB23	AK33	—	—	RX_DAT_IN_4_P	L6_A0	L6_A0
AA23	AJ32	—	—	RX_DAT_IN_4_N	L6_A0	L6_A0
AC25	AH31	—	—	RX_DAT_IN_5_P	L7_D0	L7_A0
AB24	AG30	—	—	RX_DAT_IN_5_N	L7_D0	L7_A0
AB25	AF30	—	—	RX_DAT_IN_6_P	L8_D0	L8_A0
AA24	AG31	—	—	RX_DAT_IN_6_N	L8_D0	L8_A0
AC26	AK34	—	—	RX_DAT_IN_7_P	L9_A0	L9_A0
AB26	AJ33	—	—	RX_DAT_IN_7_N	L9_A0	L9_A0
NC	PLANE	—	—	V_{DD}15	—	—
Y24	AH32	—	—	V_{DD}33	—	—
W23	AE30	—	—	LVCTAP_3	—	—
NC	PLANE	—	—	V_{DD}15	—	—
AA25	AG32	—	—	RX_CLK_IN_1_P	L10_A0	L10_A0
AA26	AF31	—	—	RX_CLK_IN_1_N	L10_A0	L10_A0
NC	AF32	—	—	V_{DD}33	—	—
Y23	AC30	—	—	RX_DAT_IN_8_P	L11_D0	L11_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
W24	AD30	—	—	RX_DAT_IN_8_N	L11_D0	L11_A0
NC	PLANE	—	—	V_{DD}15	—	—
Y25	AE31	—	—	RX_DAT_IN_9_P	L12_A0	L12_A0
Y26	AE32	—	—	RX_DAT_IN_9_N	L12_A0	L12_A0
NC	AF33	—	—	V_{DD}33	—	—
W25	AD31	—	—	RX_DAT_IN_10_P	L13_D0	L13_A0
V24	AD32	—	—	RX_DAT_IN_10_N	L13_D0	L13_A0
NC	PLANE	—	—	V_{DD}15	—	—
W26	AB30	—	—	LVCTAP_4	—	—
V23	AC31	—	—	RX_DAT_IN_11_P	L14_A0	L14_A0
U23	AC32	—	—	RX_DAT_IN_11_N	L14_A0	L14_A0
NC	AC33	—	—	V_{DD}33	—	—
V25	AB31	—	—	RX_CLK_IN_2_P	L15_D0	L15_A0
U24	AB32	—	—	RX_CLK_IN_2_N	L15_D0	L15_A0
V26	AA30	—	—	LVCTAP_5	—	—
NC	PLANE	—	—	V_{DD}15	—	—
U26	AB33	—	—	V_{DD}33	—	—
U25	AA31	—	—	RX_CLK_IN_3_P	L16_D0	L16_A0
T24	Y30	—	—	RX_CLK_IN_3_N	L16_D0	L16_A0
R23	AA32	—	—	RX_DAT_IN_12_P	L17_A0	L17_A0
T23	AA33	—	—	RX_DAT_IN_12_N	L17_A0	L17_A0
NC	PLANE	—	—	V_{DD}15	—	—
T25	Y31	—	—	RX_DAT_IN_13_P	L18_A0	L18_A0
T26	Y32	—	—	RX_DAT_IN_13_N	L18_A0	L18_A0
NC	W30	—	—	V_{DD}33	—	—
NC	Y33	—	—	V_{DD}33	—	—
R24	W31	—	—	RX_DAT_IN_14_P	L19_A0	L19_A0
R25	W32	—	—	RX_DAT_IN_14_N	L19_A0	L19_A0
R26	V30	—	—	RX_DAT_IN_15_P	L20_D0	L20_A0
P25	V31	—	—	RX_DAT_IN_15_N	L20_D0	L20_A0
P24	W33	—	—	V_{DD}33	—	—
P26	V32	—	—	LV_REF10	—	—
N26	V33	—	—	LV_REF14	—	—
N23	U33	—	—	LV_RESHI	—	—
P23	U31	—	—	LV_RESLO	—	—
NC	U30	—	—	V_{DD}33	—	—
NC	PLANE	—	—	V_{DD}15	—	—
N25	U32	—	—	TX_CLK_OUT_0_P	L21_A0	L21_A0
N24	T33	—	—	TX_CLK_OUT_0_N	L21_A0	L21_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	T32	—	—	$V_{DD}33$	—	—
M26	T31	—	—	TX_DAT_OUT_0_P	L22_A0	L22_A0
M25	T30	—	—	TX_DAT_OUT_0_N	L22_A0	L22_A0
M24	R33	—	—	TX_DAT_OUT_1_P	L23_A0	L23_A0
M23	R32	—	—	TX_DAT_OUT_1_N	L23_A0	L23_A0
NC	PLANE	—	—	$V_{DD}15$	—	—
L26	R31	—	—	TX_DAT_OUT_2_P	L24_A0	L24_A0
L25	R30	—	—	TX_DAT_OUT_2_N	L24_A0	L24_A0
NC	P33	—	—	$V_{DD}33$	—	—
L23	P32	—	—	TX_DAT_OUT_3_N	L25_A0	L25_A0
L24	N33	—	—	TX_DAT_OUT_3_P	L25_A0	L25_A0
K25	P31	—	—	TX_CLK_OUT_1_N	L26_D0	L26_A0
J26	P30	—	—	TX_CLK_OUT_1_P	L26_D0	L26_A0
J25	N32	—	—	TX_DAT_OUT_4_P	L27_D0	L27_A0
K24	N31	—	—	TX_DAT_OUT_4_N	L27_D0	L27_A0
NC	PLANE	—	—	$V_{DD}15$	—	—
K26	N30	—	—	$V_{DD}33$	—	—
H26	M33	—	—	TX_DAT_OUT_5_P	L28_A0	L28_A0
G26	M32	—	—	TX_DAT_OUT_5_N	L28_A0	L28_A0
K23	M31	—	—	TX_DAT_OUT_6_P	L29_A0	L29_A0
J23	M30	—	—	TX_DAT_OUT_6_N	L29_A0	L29_A0
NC	L33	—	—	$V_{DD}33$	—	—
NC	PLANE	—	—	$V_{DD}15$	—	—
J24	L32	—	—	TX_DAT_OUT_7_P	L30_D0	L30_A0
H25	K32	—	—	TX_DAT_OUT_7_N	L30_D0	L30_A0
G25	L31	—	—	TX_CLK_OUT_2_N	L31_D0	L31_A0
H24	L30	—	—	TX_CLK_OUT_2_P	L31_D0	L31_A0
F26	K31	—	—	TX_DAT_OUT_8_N	L32_A0	L32_A0
E26	J31	—	—	TX_DAT_OUT_8_P	L32_A0	L32_A0
NC	K30	—	—	$V_{DD}33$	—	—
H23	J32	—	—	TX_DAT_OUT_9_N	L33_D0	L33_A0
G24	H33	—	—	TX_DAT_OUT_9_P	L33_D0	L33_A0
G23	H32	—	—	$V_{DD}33$	—	—
F25	H31	—	—	TX_CLK_IN_P	L34_A0	L34_A0
E25	J30	—	—	TX_CLK_IN_N	L34_A0	L34_A0
F24	G32	—	—	LVCTAP_6	—	—
D26	G31	—	—	TX_DAT_OUT_10_P	L35_A0	L35_A0
D25	F32	—	—	TX_DAT_OUT_10_N	L35_A0	L35_A0
NC	H30	—	—	$V_{DD}33$	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
C25	E33	—	—	TX_DAT_OUT_11_P	L36_D0	L36_A0
D24	E32	—	—	TX_DAT_OUT_11_N	L36_D0	L36_A0
F23	F31	—	—	TX_CLK_OUT_3_P	L37_D0	L37_A0
E24	E31	—	—	TX_CLK_OUT_3_N	L37_D0	L37_A0
NC	G30	—	—	V_{DD}33	—	—
NC	PLANE	—	—	V_{DD}15	—	—
C26	F30	—	—	V_{DD}33	—	—
B25	E30	—	—	V_{SS}A_6	—	—
E23	B32	—	—	V_{DD}33	—	—
C24	C31	—	—	V_{DD}33A_6	—	—
D23	E29	—	—	V_{DD}33A_7	—	—
NC	PLANE	—	—	V_{DD}15	—	—
B24	E28	—	—	V_{SS}A_7	—	—
D22	A32	—	—	TX_DAT_OUT_12_N	L38_D0	L38_A0
C23	B31	—	—	TX_DAT_OUT_12_P	L38_D0	L38_A0
A24	E27	—	—	TX_DAT_OUT_13_N	L39_D0	L39_A0
B23	E26	—	—	TX_DAT_OUT_13_P	L39_D0	L39_A0
D21	D29	—	—	TX_DAT_OUT_14_N	L40_A0	L40_A0
NC	PLANE	—	—	V_{DD}15	—	—
C22	B30	—	—	V_{DD}33	—	—
C21	C29	—	—	TX_DAT_OUT_14_P	L40_A0	L40_A0
A23	C28	—	—	TX_DAT_OUT_15_N	L41_D0	L41_A0
B22	D27	—	—	TX_DAT_OUT_15_P	L41_D0	L41_A0
A22	A30	—	—	PWRDN	—	—
B21	E25	—	—	RESET_RX	—	—
D20	B29	—	—	RESET_TX	—	—
D19	A29	—	—	PLL_BYPASS	—	—
NC	C27	V_{DDIO}1_TC	9	PT32D	—	—
C20	D26	V_{DDIO}1_TC	9	PT32C	—	—
B20	B28	V_{DDIO}1_TC	1	PT31D	L1C_D0	L1C_A0
C19	A28	V_{DDIO}1_TC	1	PT31C/VREF_TC_10	L1T_D0	L1T_A0
NC	PLANE	—	—	V_{DD}15	—	—
NC	B27	V_{DDIO}1_TC	1	PT30D	—	—
NC	C26	V_{DDIO}1_TC	1	PT30A	—	—
A21	B26	V_{DDIO}1_TC	1	PT29D	L2C_A0	L2C_A0
A20	A27	V_{DDIO}1_TC	1	PT29C	L2T_A0	L2T_A0
L13	PLANE	—	—	V_{DD}15	—	—
NC	D25	V_{DDIO}1_TC	1	PT29A	—	L3T_A0
NC	E24	V_{DDIO}1_TC	1	PT29B	—	L3C_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
B19	D24	V_{DDIO}1_TC	1	PT28D	L3C_D0	L4C_A0
C18	C25	V_{DDIO}1_TC	1	PT28C	L3T_D0	L4T_A0
NC	A26	V_{DDIO}1_TC	1	PT28A	—	L5T_A0
NC	B25	V_{DDIO}1_TC	1	PT28B	—	L5C_A0
D18	E23	V_{DDIO}1_TC	1	PT27D/VREF_TC_01	L4C_A0	L6C_A0
D17	D23	V_{DDIO}1_TC	1	PT27C	L4T_A0	L6T_A0
B18	C24	V_{DDIO}1_TC	1	PT27B	L5C_D0	L7C_D1
C17	A25	V_{DDIO}1_TC	1	PT27A	L5T_D0	L7T_D1
A18	E22	V_{DDIO}1_TC	2	PT26D	L6C_D0	L8C_A0
B17	E21	V_{DDIO}1_TC	2	PT26C/VREF_TC_02	L6T_D0	L8T_A0
NC	B24	V_{DDIO}1_TC	2	PT26B	—	L9C_D1
NC	D22	V_{DDIO}1_TC	2	PT26A	—	L9T_D1
A17	B23	V_{DDIO}1_TC	2	PT25D	L7C_D0	L10C_A0
B16	A23	V_{DDIO}1_TC	2	PT25C	L7T_D0	L10T_A0
D16	D21	V_{DDIO}1_TC	3	PT24D	L8C_A0	L11C_D1
C16	B22	V_{DDIO}1_TC	3	PT24C/VREF_TC_03	L8T_A0	L11T_D1
NC	A22	V_{DDIO}1_TC	3	PT24A	—	—
A16	D20	V_{DDIO}1_TC	3	PT23D	L9C_A0	L12C_A0
A15	E20	V_{DDIO}1_TC	3	PT23C	L9T_A0	L12T_A0
NC	C21	V_{DDIO}1_TC	3	PT23A	—	—
NC	B21	V_{DDIO}1_TC	3	PT22D	—	L13C_A0
NC	A21	V_{DDIO}1_TC	3	PT22C	—	L13T_A0
NC	B20	V_{DDIO}1_TC	3	PT22A	—	—
C15	C19	V_{DDIO}1_TC	4	PT21D	L10C_A0	L14C_D1
C14	A20	V_{DDIO}1_TC	4	PT21C	L10T_A0	L14T_D1
L14	PLANE	—	—	V_{DD}15	—	—
NC	D19	V_{DDIO}1_TC	4	PT20D	—	L15C_A0
NC	E19	V_{DDIO}1_TC	4	PT20C	—	L15T_A0
B14	B19	V_{DDIO}1_TC	4	PT19D	L11C_A0	L16C_A0
A14	B18	V_{DDIO}1_TC	4	PT19C/VREF_TC_04	L11T_A0	L16T_A0
NC	E18	V_{DDIO}1_TC	4	PT19A	—	L17T_A0
NC	D18	V_{DDIO}1_TC	4	PT19B	—	L17C_A0
D13	B17	V_{DDIO}1_TC	5	PT18D/PTCK1C	L12C_A0	L18C_A0
C13	C17	V_{DDIO}1_TC	5	PT18C/PTCK1T	L12T_A0	L18T_A0
NC	C18	V_{DDIO}1_TC	5	PT18A	—	L19T_A0
NC	D17	V_{DDIO}1_TC	5	PT18B	—	L19C_A0
B13	A16	V_{DDIO}1_TC	5	PT17D/PTCK0C	L13C_A0	L20C_A0
A13	B16	V_{DDIO}1_TC	5	PT17C/PTCK0T	L13T_A0	L20T_A0
NC	E17	V_{DDIO}1_TC	5	PT17A	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
A12	C16	V_{DDIO}1_TC	5	PT16D/VREF_TC_05	L14C_A0	L21C_A0
B12	D16	V_{DDIO}1_TC	5	PT16C	L14T_A0	L21T_A0
NC	A15	V_{DDIO}1_TC	5	PT16A	—	—
C12	B15	V_{DDIO}1_TC	6	PT15D	L15C_A0	L22C_A1
D12	D15	V_{DDIO}1_TC	6	PT15C	L15T_A0	L22T_A1
NC	A14	V_{DDIO}1_TC	6	PT15A	—	—
B11	E16	V_{DDIO}1_TC	6	PT14D	L16C_A0	L23C_D1
A11	C14	V_{DDIO}1_TC	6	PT14C/VREF_TC_06	L16T_A0	L23T_D1
NC	B14	V_{DDIO}1_TC	6	PT14A	—	—
D11	E15	V_{DDIO}0_TL	1	PT13D/$\overline{\text{MPI_RTRY}}$	L1C_A0	L1C_A0
C11	D14	V_{DDIO}0_TL	1	PT13C/$\overline{\text{MPI_ACK}}$	L1T_A0	L1T_A0
NC	A13	V_{DDIO}0_TL	1	PT13B	—	L2C_A0
C10	B13	V_{DDIO}0_TL	1	PT13A/VREF_TL_01	—	L2T_A0
B10	A12	V_{DDIO}0_TL	1	PT12D/M0	L2C_D0	L3C_A0
A9	B12	V_{DDIO}0_TL	1	PT12C/M1	L2T_D0	L3T_A0
B9	D13	V_{DDIO}0_TL	2	PT12B/MPI_CLK	L3C_A0	L4C_A0
C9	E14	V_{DDIO}0_TL	2	PT12A/A21/$\overline{\text{MPI_BURST}}$	L3T_A0	L4T_A0
D10	B11	V_{DDIO}0_TL	2	PT11D/M2	L4C_A0	L5C_A0
D9	A10	V_{DDIO}0_TL	2	PT11C/M3	L4T_A0	L5T_A0
A8	E13	V_{DDIO}0_TL	2	PT11B/VREF_TL_02	L5C_A0	L6C_A0
B8	D12	V_{DDIO}0_TL	2	PT11A/$\overline{\text{MPI_TEA}}$	L5T_A0	L6T_A0
NC	C11	V_{DDIO}0_TL	3	PT10D	—	L7C_A0
NC	B10	V_{DDIO}0_TL	3	PT10C	—	L7T_A0
NC	A9	V_{DDIO}0_TL	3	PT10A	—	—
K13	PLANE	—	—	V_{DD}15	—	—
A7	D11	V_{DDIO}0_TL	3	PT9D/VREF_TL_03	L6C_A0	L8C_D1
A6	B9	V_{DDIO}0_TL	3	PT9C	L6T_A0	L8T_D1
NC	A8	V_{DDIO}0_TL	3	PT9A	—	—
C8	E12	V_{DDIO}0_TL	3	PT8D/D0/DIN	L7C_D0	L9C_D1
B7	C10	V_{DDIO}0_TL	3	PT8C/TMS	L7T_D0	L9T_D1
C7	D10	V_{DDIO}0_TL	4	PT7D/A20/$\overline{\text{MPI_BDIP}}$	L8C_D0	L10C_A0
B6	C9	V_{DDIO}0_TL	4	PT7C/A19/MPI_TSZ1	L8T_D0	L10T_A0
D7	E11	V_{DDIO}0_TL	4	PT6D/A18/MPI_TSZ0	L9C_A0	L11C_D1
D8	D9	V_{DDIO}0_TL	4	PT6C/D3	L9T_A0	L11T_D1
NC	A7	V_{DDIO}0_TL	4	PT6B/VREF_TL_04	—	L12C_A0
NC	B8	V_{DDIO}0_TL	4	PT6A	—	L12T_A0
C6	E10	V_{DDIO}0_TL	5	PT5D/D1	L10C_D0	L13C_D1
B5	C8	V_{DDIO}0_TL	5	PT5C/D2	L10T_D0	L13T_D1
NC	B7	V_{DDIO}0_TL	5	PT5B	—	L14C_A0

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	A6	V_{DDIO}0_TL	5	PT5A/VREF_TL_05	—	L14T_A0
A4	D8	V_{DDIO}0_TL	5	PT4D/TDI	L11C_D1	L15C_D1
NC	C7	V_{DDIO}0_TL	5	PT4B	—	L16C_D1
C5	B6	V_{DDIO}0_TL	5	PT4C/TCK	L11T_D1	L15T_D1
NC	A5	V_{DDIO}0_TL	5	PT4A	—	L16T_D1
B3	C6	V_{DDIO}0_TL	6	PT3D	L12C_A0	L17C_A0
NC	E9	V_{DDIO}0_TL	6	PT3B	—	L18C_D1
A3	B5	V_{DDIO}0_TL	6	PT3C/VREF_TL_06	L12T_A0	L17T_A0
NC	D7	V_{DDIO}0_TL	6	PT3A	—	L18T_D1
D5	C5	V_{DDIO}0_TL	6	PT2D/PLL_CK1C	L13C_A0	L19C_A0
D6	D6	V_{DDIO}0_TL	6	PT2C/PLL_CK1T	L13T_A0	L19T_A0
NC	E8	V_{DDIO}0_TL	6	PT2B	—	L20C_A0
NC	E7	V_{DDIO}0_TL	6	PT2A	—	L20T_A0
B4	A4	V_{DDIO}0_TL	—	PCFG_MPI_IRQ/$\overline{\text{CFG_IRQ}}$/$\overline{\text{MPI_IRQ}}$	—	—
B2	B4	—	—	PCCLK	—	—
K14	PLANE	—	—	V_{DD}15	—	—
C4	E6	—	—	PDONE	—	—
C3	D5	—	—	V_{DD}33	—	—
M14	A31	—	—	V_{DD}15	—	—
N10	C30	—	—	V_{DD}15	—	—
N11	C33	—	—	V_{DD}15	—	—
N12	C34	—	—	V_{DD}15	—	—
N15	D28	—	—	V_{DD}15	—	—
N16	D32	—	—	V_{DD}15	—	—
N17	D34	—	—	V_{DD}15	—	—
P10	F34	—	—	V_{DD}15	—	—
P11	G33	—	—	V_{DD}15	—	—
P12	G34	—	—	V_{DD}15	—	—
M13	J34	—	—	V_{DD}15	—	—
P15	K33	—	—	V_{DD}15	—	—
NC	K34	—	—	V_{DD}15	—	—
NC	M34	—	—	V_{DD}15	—	—
NC	N16	—	—	V_{DD}15	—	—
NC	N17	—	—	V_{DD}15	—	—
P17	N18	—	—	V_{DD}15	—	—
AF1	N19	—	—	V_{DD}15	—	—
NC	N34	—	—	V_{DD}15	—	—
NC	P16	—	—	V_{DD}15	—	—
NC	P17	—	—	V_{DD}15	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	P18	—	—	V_{DD}15	—	—
NC	P19	—	—	V_{DD}15	—	—
NC	R16	—	—	V_{DD}15	—	—
NC	R17	—	—	V_{DD}15	—	—
NC	R18	—	—	V_{DD}15	—	—
NC	R19	—	—	V_{DD}15	—	—
NC	R34	—	—	V_{DD}15	—	—
NC	T13	—	—	V_{DD}15	—	—
NC	T14	—	—	V_{DD}15	—	—
NC	T15	—	—	V_{DD}15	—	—
NC	T20	—	—	V_{DD}15	—	—
NC	T21	—	—	V_{DD}15	—	—
NC	T22	—	—	V_{DD}15	—	—
NC	T34	—	—	V_{DD}15	—	—
NC	U13	—	—	V_{DD}15	—	—
NC	U14	—	—	V_{DD}15	—	—
NC	U15	—	—	V_{DD}15	—	—
NC	U20	—	—	V_{DD}15	—	—
NC	U21	—	—	V_{DD}15	—	—
NC	U22	—	—	V_{DD}15	—	—
NC	V13	—	—	V_{DD}15	—	—
NC	V14	—	—	V_{DD}15	—	—
NC	V15	—	—	V_{DD}15	—	—
NC	V20	—	—	V_{DD}15	—	—
NC	V21	—	—	V_{DD}15	—	—
NC	V22	—	—	V_{DD}15	—	—
NC	V34	—	—	V_{DD}15	—	—
NC	W13	—	—	V_{DD}15	—	—
NC	W14	—	—	V_{DD}15	—	—
NC	W15	—	—	V_{DD}15	—	—
NC	W20	—	—	V_{DD}15	—	—
NC	W21	—	—	V_{DD}15	—	—
NC	W22	—	—	V_{DD}15	—	—
NC	W34	—	—	V_{DD}15	—	—
NC	Y16	—	—	V_{DD}15	—	—
NC	Y17	—	—	V_{DD}15	—	—
NC	Y18	—	—	V_{DD}15	—	—
NC	Y19	—	—	V_{DD}15	—	—
NC	AA16	—	—	V_{DD}15	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	AA17	—	—	V_{DD}15	—	—
NC	AA18	—	—	V_{DD}15	—	—
NC	AA19	—	—	V_{DD}15	—	—
NC	AA34	—	—	V_{DD}15	—	—
NC	AB16	—	—	V_{DD}15	—	—
NC	AB17	—	—	V_{DD}15	—	—
NC	AB18	—	—	V_{DD}15	—	—
NC	AB19	—	—	V_{DD}15	—	—
NC	AB34	—	—	V_{DD}15	—	—
NC	AD33	—	—	V_{DD}15	—	—
NC	AD34	—	—	V_{DD}15	—	—
NC	AE34	—	—	V_{DD}15	—	—
NC	AG33	—	—	V_{DD}15	—	—
NC	AG34	—	—	V_{DD}15	—	—
NC	AH34	—	—	V_{DD}15	—	—
NC	AK29	—	—	V_{DD}15	—	—
NC	AL32	—	—	V_{DD}15	—	—
NC	AL33	—	—	V_{DD}15	—	—
NC	AL34	—	—	V_{DD}15	—	—
NC	AM31	—	—	V_{DD}15	—	—
NC	AM33	—	—	V_{DD}15	—	—
NC	AM34	—	—	V_{DD}15	—	—
NC	AN32	—	—	V_{DD}15	—	—
NC	AP31	—	—	V_{DD}15	—	—
A2	A1	—	—	V_{SS}	—	—
A25	A18	—	—	V_{SS}	—	—
B1	A33	—	—	V_{SS}	—	—
NC	A34	—	—	V_{SS}	—	—
NC	B2	—	—	V_{SS}	—	—
NC	B33	—	—	V_{SS}	—	—
U16	B34	—	—	V_{SS}	—	—
U17	C3	—	—	V_{SS}	—	—
AE1	C13	—	—	V_{SS}	—	—
AE26	C22	—	—	V_{SS}	—	—
AF2	C32	—	—	V_{SS}	—	—
AF25	D4	—	—	V_{SS}	—	—
NC	D30	—	—	V_{SS}	—	—
NC	D31	—	—	V_{SS}	—	—
NC	D33	—	—	V_{SS}	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	E34	—	—	Vss	—	—
T16	F33	—	—	Vss	—	—
T17	H34	—	—	Vss	—	—
U10	J33	—	—	Vss	—	—
U11	L34	—	—	Vss	—	—
U12	N13	—	—	Vss	—	—
U15	N14	—	—	Vss	—	—
NC	N15	—	—	Vss	—	—
NC	N20	—	—	Vss	—	—
NC	N21	—	—	Vss	—	—
NC	N22	—	—	Vss	—	—
NC	P13	—	—	Vss	—	—
NC	P14	—	—	Vss	—	—
NC	P15	—	—	Vss	—	—
R16	P20	—	—	Vss	—	—
R17	P21	—	—	Vss	—	—
T10	P22	—	—	Vss	—	—
T11	P34	—	—	Vss	—	—
T12	R13	—	—	Vss	—	—
T15	R14	—	—	Vss	—	—
NC	R15	—	—	Vss	—	—
NC	R20	—	—	Vss	—	—
NC	R21	—	—	Vss	—	—
NC	R22	—	—	Vss	—	—
NC	T16	—	—	Vss	—	—
NC	T17	—	—	Vss	—	—
K12	T18	—	—	Vss	—	—
K15	T19	—	—	Vss	—	—
K16	U16	—	—	Vss	—	—
K17	U17	—	—	Vss	—	—
L10	U18	—	—	Vss	—	—
L11	U19	—	—	Vss	—	—
NC	U34	—	—	Vss	—	—
NC	V16	—	—	Vss	—	—
NC	V17	—	—	Vss	—	—
NC	V18	—	—	Vss	—	—
NC	V19	—	—	Vss	—	—
NC	W16	—	—	Vss	—	—
NC	W17	—	—	Vss	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	W18	—	—	Vss	—	—
NC	W19	—	—	Vss	—	—
NC	Y13	—	—	Vss	—	—
NC	Y14	—	—	Vss	—	—
B26	Y15	—	—	Vss	—	—
K10	Y20	—	—	Vss	—	—
K11	Y21	—	—	Vss	—	—
NC	Y22	—	—	Vss	—	—
L12	Y34	—	—	Vss	—	—
L15	AA13	—	—	Vss	—	—
L16	AA14	—	—	Vss	—	—
L17	AA15	—	—	Vss	—	—
M10	AA20	—	—	Vss	—	—
M11	AA21	—	—	Vss	—	—
M12	AA22	—	—	Vss	—	—
M15	AB13	—	—	Vss	—	—
M16	AB14	—	—	Vss	—	—
M17	AB15	—	—	Vss	—	—
N13	AB20	—	—	Vss	—	—
N14	AB21	—	—	Vss	—	—
P13	AB22	—	—	Vss	—	—
P14	AC34	—	—	Vss	—	—
R10	AE33	—	—	Vss	—	—
R11	AF34	—	—	Vss	—	—
R12	AH33	—	—	Vss	—	—
R15	AJ34	—	—	Vss	—	—
NC	AL2	—	—	Vss	—	—
NC	AL4	—	—	Vss	—	—
NC	AL30	—	—	Vss	—	—
NC	AL31	—	—	Vss	—	—
NC	AM3	—	—	Vss	—	—
NC	AM13	—	—	Vss	—	—
NC	AM22	—	—	Vss	—	—
NC	AM32	—	—	Vss	—	—
NC	AN2	—	—	Vss	—	—
NC	AN33	—	—	Vss	—	—
NC	AN34	—	—	Vss	—	—
NC	AP1	—	—	Vss	—	—
NC	AP4	—	—	Vss	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
NC	AP33	—	—	V_{SS}	—	—
NC	AP34	—	—	V_{SS}	—	—
C2	A2	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	A3	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	B1	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
G3	B3	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	C2	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
A10	C4	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	D2	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	D3	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
A5	E1	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	E3	V_{DDIO}0_TL	—	V_{DDIO}0_TL	—	—
NC	A11	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
NC	A17	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
NC	A19	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
A19	A24	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
D15	C12	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
B15	C15	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
D14	C20	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
NC	C23	V_{DDIO}1_TC	—	V_{DDIO}1_TC	—	—
AF14	AM12	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
AF16	AM15	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
AF17	AM20	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
AD17	AM23	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
NC	AP11	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
AD20	AP17	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
NC	AP19	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
NC	AP24	V_{DDIO}5_BC	—	V_{DDIO}5_BC	—	—
NC	AK4	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
AB1	AK5	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
NC	AL1	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
NC	AL3	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
AD2	AM1	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
NC	AM2	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
NC	AM4	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
AF5	AN3	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
AF9	AP2	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
NC	AP3	V_{DDIO}6_BL	—	V_{DDIO}6_BL	—	—
K1	L1	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—

Pin Information (continued)

Table 19. PBGA Pinout Table (continued)

416 BGA Ball	680 BGA Ball	V_{DDIO} Bank	V_{REF} Group	ORLI10G Pin Description	416 BGA Pair	680 BGA Pair
L2	M3	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—
NC	R3	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—
P2	U1	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—
NC	W1	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—
T3	Y3	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—
NC	AC3	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—
NC	AD1	V_{DDIO}7_CL	—	V_{DDIO}7_CL	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: Θ_{JA}, ψ_{JC}, and Θ_{JC}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

ΘJA

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.).

$$\Theta_{JA} = \frac{T_J - T_A}{Q}$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, Θ_{JA} is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that Θ_{JA} is expressed in units of °C/watt.

ψJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by:

$$\psi_{JC} = \frac{T_J - T_C}{Q}$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the Θ_{JA} measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψ_{JC} is also expressed in units of °C/W.

ΘJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta_{JC} = \frac{T_J - T_C}{Q}$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates Θ_{JC} from ψ_{JC}. Θ_{JC} is a true thermal resistance and is expressed in units of °C/W.

ΘJB

This is the thermal resistance from junction to board (Θ_{JL}). It is defined by:

$$\Theta_{JB} = \frac{T_J - T_B}{Q}$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the righthand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that Θ_{JB} is expressed in units of °C/W, and that this parameter and the way it is measured are still in JEDEC committee.

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined (see the Estimating Power Dissipation section), the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$T_{Jmax} = T_{Amax} + (Q \bullet \Theta_{JA})$

Table 20 lists the thermal characteristics for all packages used with the *ORCA* ORLI10G FPSC.

Package Thermal Characteristics

Table 20*. ORCA* ORLI10G Plastic Package Thermal Guidelines

Package	ΘJA (°C/W)			Max Power
	0 fpm	200 fpm	500 fpm	T = 70 °C Max T_J = 125 °C Max 0 fpm (W)
416-Pin PBGAM	19.5	16.5	13.5	2.8
680-Pin PBGAM	15.5	12.5	11.5	3.5

Heat Sink Vendors for BGA Packages

The estimated worst-case power requirements for the ORLI10G with a programmable XGMII to XSBI interface for 10 Gbits/s Ethernet applications is 4.0 W. Consequently, for most applications an external heat sink will be required. Below, in alphabetical order, is a list of heat sink vendors who advertise heat sinks aimed at the BGA market.

Table 21. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermal Technology	Laconia, NH	(603) 527-2152
Chip Coolers	Warwick, RI	(800) 227-0254
IERC	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Thermalloy	Dallas, TX	(214) 243-4321
Wafefield Engineering	Wakefield, MA	(617) 246-0874

Package Coplanarity

The coplanarity limits of the Lucent packages are as follows:

- PBGAM: 8.0 mils

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 22 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 22 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 22. *ORCA* ORLI10G Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
416-Pin PBGAM	3.52	0.80	235	0.40	1.0	0.25	1.5—5.0	0.5—1.30
680-Pin PBGAM	3.80	1.30	250	0.50	1.0	0.30	2.8—5.0	0.5—1.50

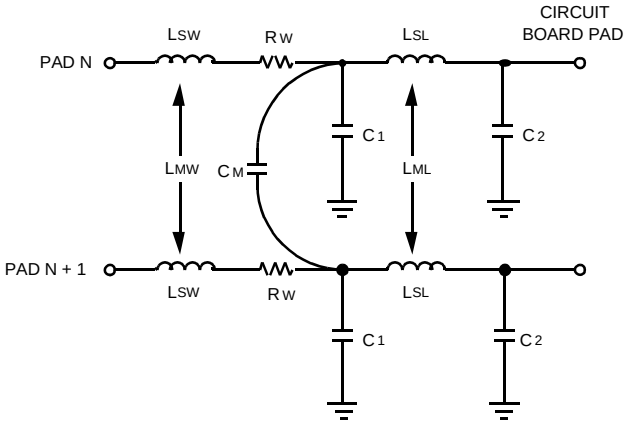


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Figure 27. Package Parasitics

Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

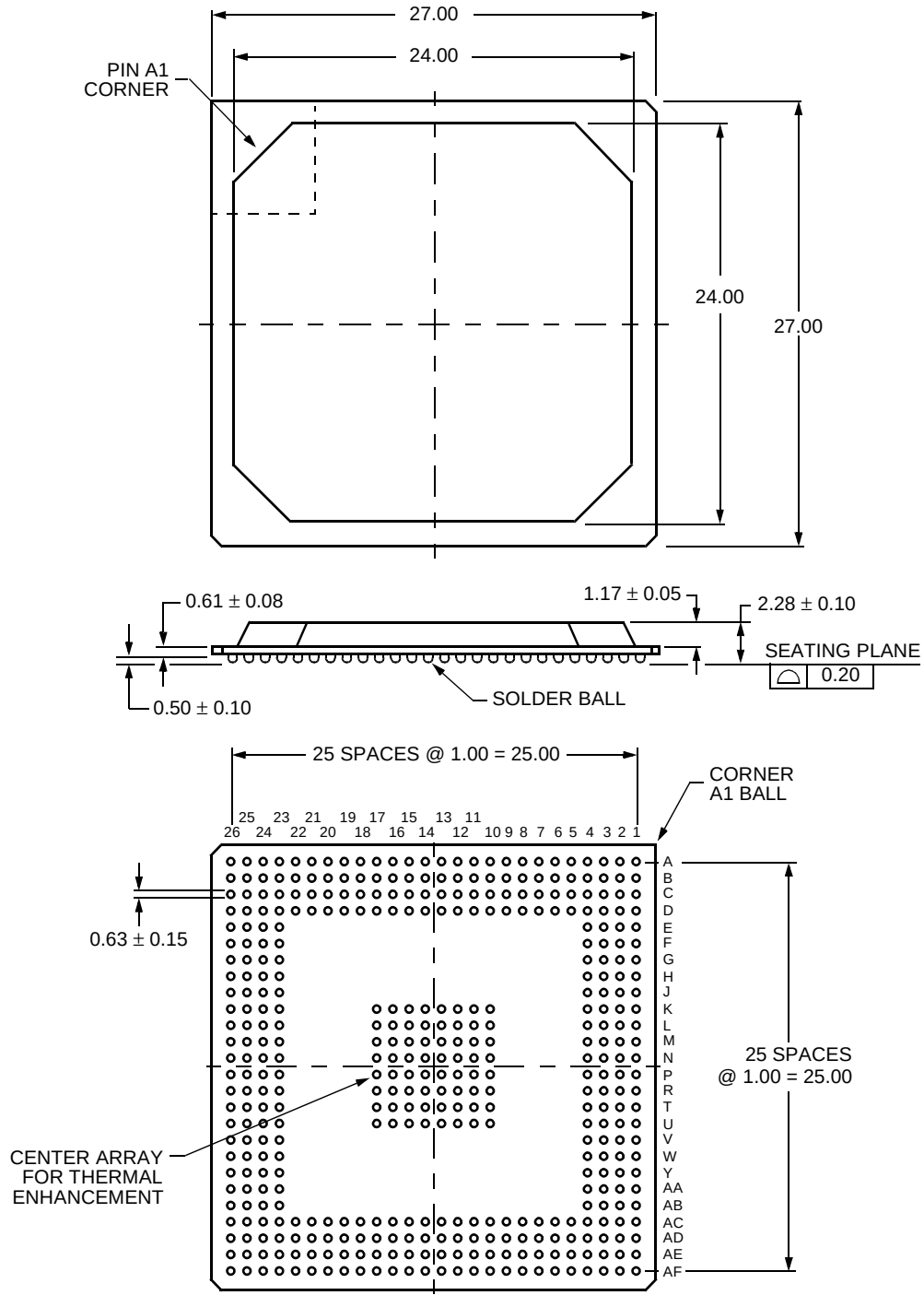
Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

Package Outline Diagrams (continued)

416-Pin PBGAM

Dimensions are in millimeters.



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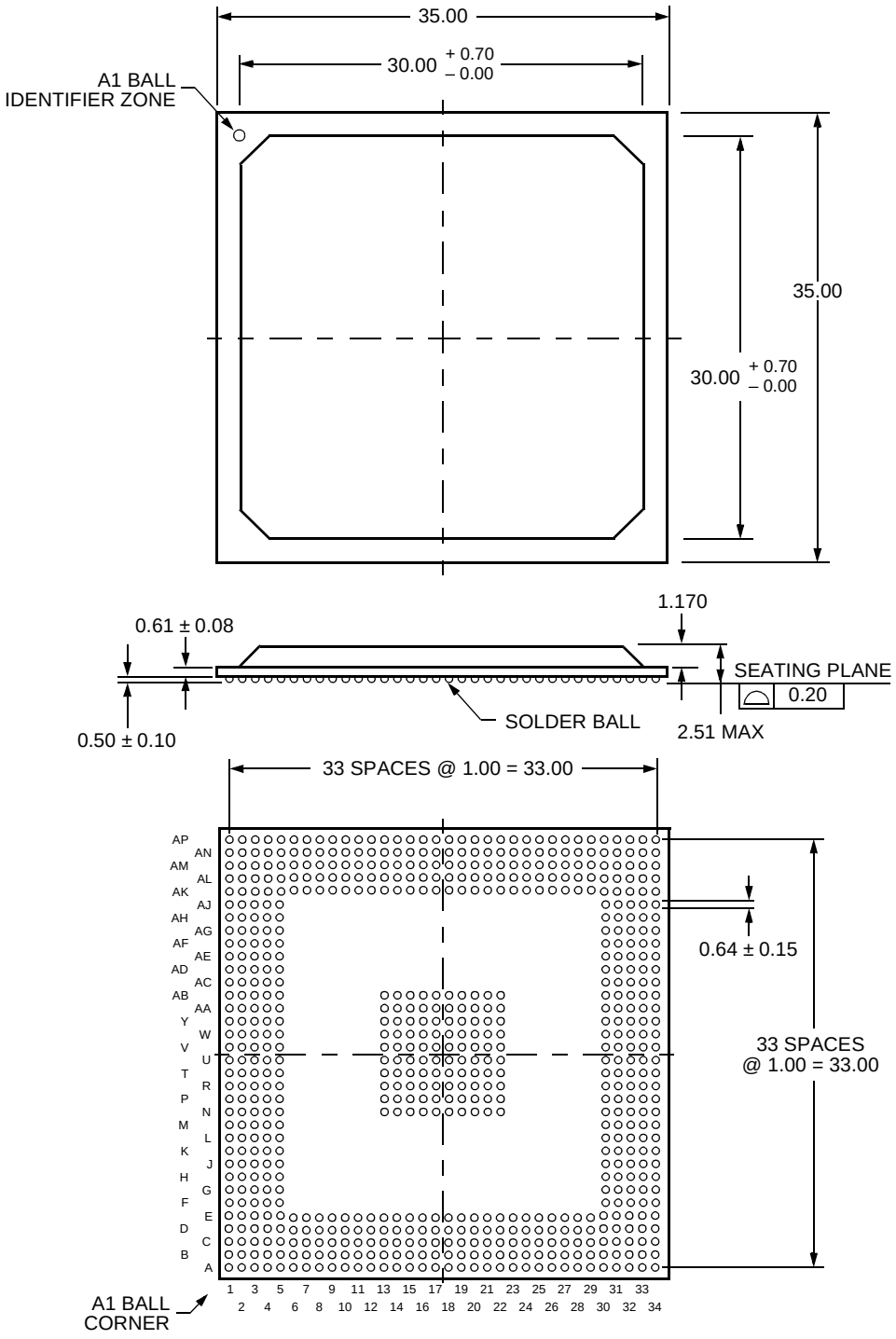
Package Outline Diagrams (continued)

680-Pin PBGAM

Dimensions are in millimeters.



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Hardware Ordering Information

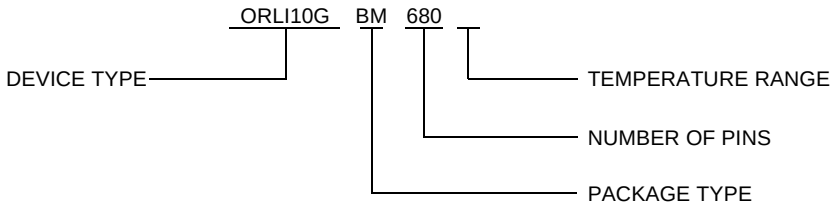

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Table 23. Device Type Options

Device	Parameter	Value
ORLI10G	Voltage	1.5 V core 3.3 V/2.5 V I/O
	Package	416-pin PBGAM (BM416) 680-pin PBGAM (BM680)

Table 24. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 25. Package Type Options

Symbol	Description
BM	Plastic Ball Grid Array, Multilayer

Table 26*. ORCA* FPSC Package Matrix (Speed Grades)

Device	Package	
	416-Pin PBGAM	680-Pin PBGAM
	BM416	BM680
ORLI10G	–1	–1

Software Ordering Information

Implementing a design in an ORLI10G requires the *ORCA* Foundry Development System and an ORLI10G FPSC Desgin Kit. For ordering information, please visit:

http://www.lucent.com/micro/netcom/ipkits/orli10g/

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Agere Systems Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Agere Systems (Shanghai) Co., Ltd., 33/F Jin Mao Tower, 88 Century Boulevard Pudong, Shanghai 200121 PRC
Tel. (86) 21 50471212, FAX (86) 21 50472266
JAPAN: Agere Systems Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 3507670** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

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